A Power-On Reset (POR) Circuit for Actel Devices

The state of a system at start-up is an important consideration in designing a circuit. It is usually desirable to provide an input signal at start-up to reset synchronous circuitry. Otherwise, the system may initially operate in an unpredictable fashion because flip-flops are not designed to power-on in any particular state. Figure 1 shows a typical power-on reset (POR) circuit from which the series resistor, R1, is omitted for TTL circuits.

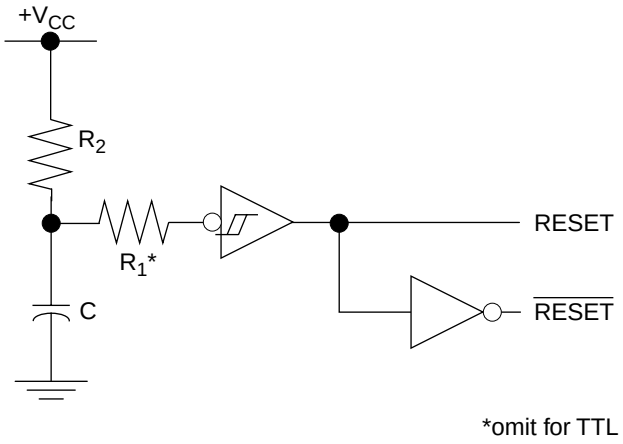

Figure 1 • *Power-On Reset Circuit*

This resistor is necessary with CMOS implementations to prevent damage to the device when power is removed from the circuit. Otherwise, the capacitor would try to power the system via the CMOS input gate protection circuit. A Schmitt trigger (40106, 74LS14) may be advantageous in making the RESET signal switch off cleanly. The hysteresis symbol shown in Figure 1 indicates an inverter with a Schmitt trigger input such as the CMOS 40106 hex inverter. The following sections describe the power-up conditions of an Actel device and a recommended POR circuit.

Behavior of ACT™ 1 FPGA Inputs

During power-on, the +5 V logic supply rail of a system typically rises from 0 to +5 V in 50 ms or less. Because regulator outputs are usually current limited during this transition, the rise time is more or less linear, with a slope in the range of 0.1 V/ms to 5 V/ms. Each Actel FPGA has a universal pad driver design that may be configured as an input, output, three-state output, or bidirectional input/output. This configuration of the pad driver is accomplished by programming antifuses in the pad driver circuitry.

As the +5 V logic supply rail passes through the region from approximately +2.2 V through +2.5 V, pad drivers that have been programmed as inputs may behave temporarily as outputs that are in the logical '1' state. Thus, these input pins will temporarily source current (approximately 8 to 10 mA, if not otherwise limited) into whatever driver is connected to them. They will be sourcing this current from the +5 V logic rail, which at this time is at +2.2 to +2.5 V. This duration is a function of the power rail rise time. For +5 V rails that come up quickly, at 5 V/ms, the duration of the behavior will be approximately 60 µs. For supply rails that rise slowly, at 0.1 V/ms, the duration of the current sourcing behavior will be 3 ms. In the former case, the Actel input can deliver as much as 0.6 µC to the circuit that drives it; in the latter case, the charge is as much as 30 µC. For many driver circuits, this amount of charge is insignificant; however, for others it may be unacceptable.

Inserting a series resistance of sufficient size into the Actel input line can limit the effect of this behavior. In the case of the POR circuit in Figure 2, the series resistance must be chosen to keep $\Delta V \leq 1V$. This guarantees that the POR remains at a logic '0' following the irregularity when the logic supply rail is at approximately 2.5 V, where $\Delta V/\Delta t = i/C$ is the voltage rise time of the capacitor. The capacitor is charged through a resistor to the 5 V logic supply rail, and the diode across the resistor is used to discharge the capacitor at power-off. For a power rail rise time of 0.1 V/ms, the duration of this behavior will be approximately 3 ms. This means that for a POR capacitance of 0.1 µF, the current out of the Actel device input must be limited to

$$i = C\Delta v / \Delta t = (0.1\ \mu F * 1\ V) / 3\ ms = 33\ \mu A$$

which can be achieved using a resistance of 2.24 V/33 mA = 68 kΩ.

Furthermore, for drivers that cannot accept a source of current at their outputs or for a multiple-source data bus, it is strongly recommended that the bus drivers be three stated during POR.

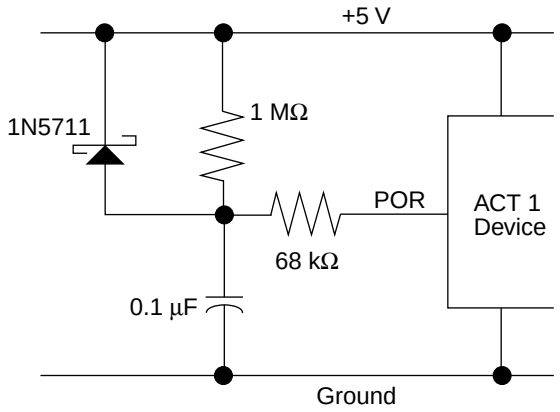

Figure 2 • *Power-On Reset (POR) Circuit with Current-Limiting Resistor*

Device Behavior during Power-Up

Actel devices have been characterized with two V_{CC} rise time conditions—fast power-up of approximately 0.5 V/µs and slow power-up of approximately 0.2 V/ms. During power-up, the following I/O conditions were characterized: input characteristics, tristate outputs, output driving low, output driving high, and output toggling. Normal input behavior is defined as the input being high impedance (<10 µA leakage). Normal output behavior means the output will either be tristate or be in a predictable state as defined by the logic of the user's design. The description that follows summarizes what happens to the Actel devices during power-up.

ACT 1 Devices

Inputs and outputs will behave normally within 100 µs after V_{CC} reaches 4.75 V with fast power-up and 3.5 V with slow power-up. With fast power-up, inputs remain in a high impedance state. With slow power-up, prior to reaching 3.5 V, inputs will momentarily behave as outputs driving high or low. This happens in about a 0.3 V window between 1 V and 2.5 V. The length of time this high or low level is exerted depends on the rise time of V_{CC}. At 0.2 V/ms, the input went high for about 1 ms and twice went low for about 150 µs each time. Tristated outputs will behave about the same as inputs. Outputs driving high or low will sometimes go to the opposite state (or tristate). Toggling outputs may not perform as expected until V_{CC} reaches 3.5 V. When V_{CC} is between 1.5 V and 3.5 V, I_{CC} will increase to 10–60 mA and then return to normal. The duration is dependant on the V_{CC} rise time, slow power-up being the worst case.

The inputs and outputs of the 3.3 V devices will behave normally within 200 µs after V_{CC} reaches 3 V for fast power-up and within 100 µs after V_{CC} reaches 2 V for slow power-up.

ACT 2/1200XL/3200DX Devices

Normal operation will occur within 100 µs after V_{CC} reaches 3.5 V for both fast and slow power-up. With slow power-up, inputs and tristated outputs will behave as outputs driving high for approximately 200 µs during a 0.3 V window where V_{CC} is between 1.5 V and 3.0 V. Inputs and tristated outputs stay at high impedance with fast power-up. I_{CC} will rise to 10–50 mA when V_{CC} is between 2 V and 4.5 V and then return to normal.

The 1200XL and 3200DX devices are expected to reach normal operation within 100 µs after V_{CC} reaches 3 V.

ACT 3/ACT 3 PCI Devices

Normal operation for inputs and outputs will occur within 100 µs after V_{CC} reaches 2.75 V. Before reaching the point of normal operation, all inputs and outputs are in a high impedance state (tristate) regardless of V_{CC} rise time. I_{CC} rises to 10–60 mA when V_{CC} is between 2 V and 3 V and then returns to normal.

Summary

Use these methods for avoiding POR problems. The transistors for these devices are turned on at approximately 0.7 V, their threshold voltage, while the circuit is functionally operational at a voltage level of approximately 3.3 V. The global routed clocks in Actel devices can also be used as resets for synchronous circuits when connected to either CLEAR or PRESET inputs of synchronous macros for the ACT 1 family, and to the CLEAR input for ACT 2, 1200XL, 3200DX, and ACT 3/ACT 3 PCI families.