Panel on System Level Design and VHDL

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VHDL in the design flow

- At the system level, specify aspects of the system
  - structure (architectural partitioning)
  - behaviour (data transforms, reactions)
  - . . .
- VHDL allows description of structure and behaviour
- Prefer single language approach
  - system level to detailed design (hardware/software)
  - aids refinement
  - avoid semantic mismatch

Problem with VHDL

- Behaviour includes concurrency and communication
- Communication performed using signals
  - assignment, resolution, waits
- Signals do not express synchronization
  - *cf.* system description and programming languages
  - assignment schedules a message for a particular time
  - receiver may miss the message
    - if it does not respond at that time

Ad hoc solutions

- Communication using handshaking protocol
  - requires extra signals
  - requires protocol implementation
- Explicitly instantiated message queues
  - extra components
- Both detract from abstraction of communication
  - introduction of extraneous artefacts

cf. other description languages

for describing behaviour, eg:

- StateCharts
- Estelle
- SDL
- CSP
- . . .

➨ Concurrent processes with message passing

Comparison with VHDL

- Concurrent process model with message passing
  ≡ concurrent FSMs communicating by events
- VHDL
  - statically specified processes & channels (signals)
  - asynchronous unbuffered message passing (?!)
- Alternatives
  - static vs. dynamic process