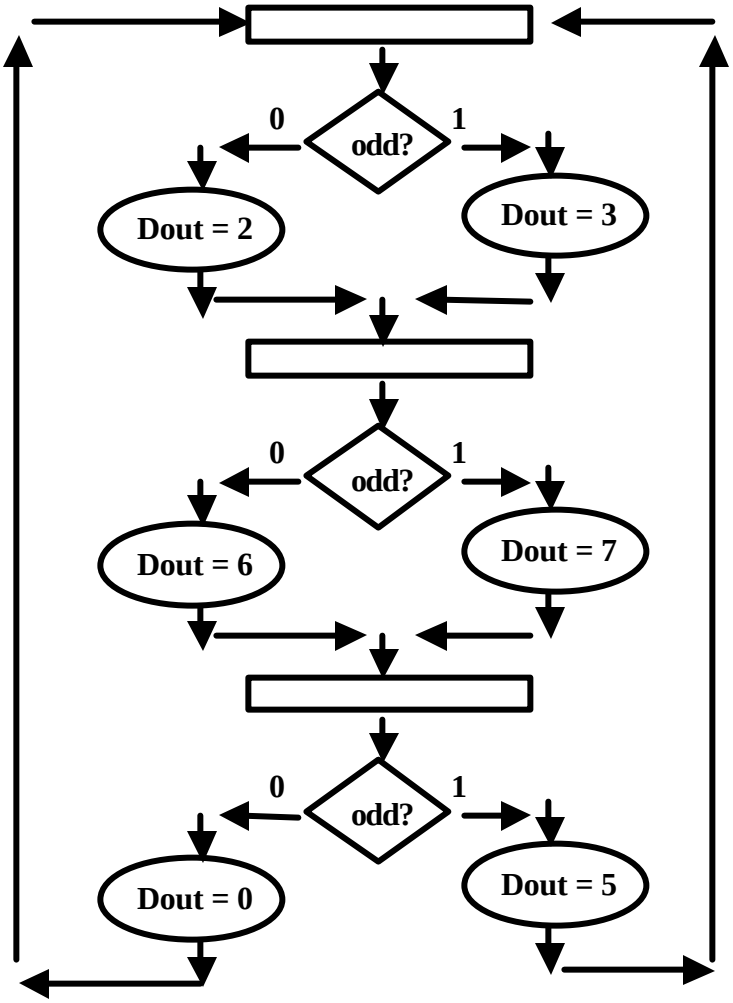
ECE 3724/CS 3124 Homework #1 Solution

This homework refers to the SSN processor discussed in Lecture #1 (EE 3724 Introduction).

1. Write and assemble a program for the SSN processor based upon YOUR Student ID number. *REFER TO INTRODUCTION LECTURE*
2. Disassemble the program below. Give the number sequence for ODD = 1, and ODD = 0. Draw an ASM chart shows the behavior of this program.

Mem Location	Mem Contents	Instruction
00	01 0011	JC loc3
01	10 0010	Out 2
02	00 0100	Jmp loc 4
03	10 0011	Out 3
04	01 0111	JC loc7
05	10 0110	Out 6
06	00 1000	Jmp loc 8
07	10 0111	Out 7
08	01 1011	Jmp loc 0B
09	10 0000	Out 0
0A	00 0000	Jmp loc 0
0B	10 0101	Out 5
0C	00 0000	Jmp loc 0

Odd sequence: 3,7,5
Even sequence: 2,6,0



3. What changes would have have to made to architecture of the SSN processor if I wanted to be able to write a program that had a maximum of 32 instructions in it? Show your work.

DATA field must be increased from 4-bits to 5-bits to support 32 instructions ($2^5 = 32$).
OP code field remains the same since the number of distinct instruction types (JC, JMP, OUT) has not changed.
Total word size (Opcode + Data) increases from 6 bits to 7 bits.
Memory size changes from 16 x 6 to 32 x 7.
Instruction Pointer implemented by the counter must increase from a 4-bit counter to a 5-bit counter.