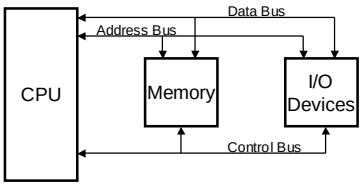
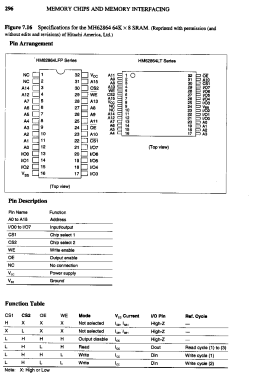
Modern Computer Model



- CPU - Central Processing Unit
  - arithmetic, logical, synchronization functions
- Memory - Stores Information
  - CPU instructions and Data
- I/O - Input/Output Devices - Peripherals
  - Interface to Outside World (humans, other machines)
- Bus - Set of Parallel wires
  - Transmit instructions/data between CPU/Memory/IO

SRAM Pinout (p. 296)



296 MEMORY CHIPS AND MEMORY INTERFACING

Figure 7.16 Specifications for the MH62864-64K × 8 SRAM. (Reprinted with permission (and without edits and revisions) of Hitachi America, Ltd.)

Pin Arrangement

Pin Description

Pin Name	Function
A0 to A15	Address
I/O0 to I/O7	Input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Function Table

CS1	CS2	OE	WE	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: High or Low

SRAM Timing Specs (p. 297)

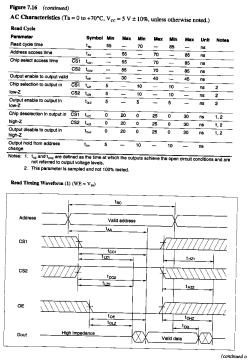


Figure 7.16 (continued)

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Read Cycle

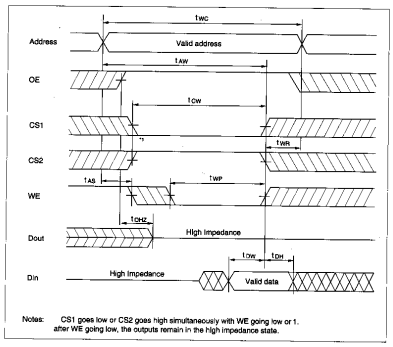
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time		t_{RC}	55	—	70	—	85	—	ns	
Address access time		t_{AA}	—	55	—	70	—	85	ns	
Chip select access time	CS1	t_{ACS1}	—	55	—	70	—	85	ns	
	CS2	t_{ACS2}	—	55	—	70	—	85	ns	
Output enable to output valid		t_{OE}	—	30	—	40	—	45	ns	
Chip selection to output in low-Z	CS1	t_{CLZ1}	5	—	10	—	10	—	ns	2
	CS2	t_{CLZ2}	5	—	10	—	10	—	ns	2
Output enable to output in low-Z		t_{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	CS1	t_{CHZ1}	0	20	0	25	0	30	ns	1, 2
	CS2	t_{CHZ2}	0	20	0	25	0	30	ns	1, 2
Output disable to output in high-Z		t_{OHZ}	0	20	0	25	0	30	ns	1, 2
Output hold from address change		t_{OH}	5	—	10	—	10	—	ns	

Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.

Read Timing Waveform (1) (WE = V_{IH})

(continued)

SRAM Timing Specs (p. 298)



HM62864 Signals (64×8)

$\overline{CS1}$, CS2 - Chip Select
– *"turn the chip on"*

$\overline{OE}$ - Output Enable
– *enable output tri-state buffers*

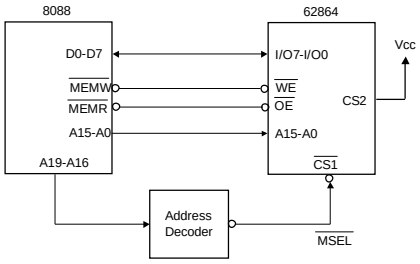
$\overline{WE}$ - Write Enable
– *enable data input tri-state buffers*

A0-A15 - 16 Address Lines
– *"point to a 1-byte value"*

I/O0-I/O7 - 8 Data Lines

8088 Memory Interface

(8-bit Data Bus)



- *8088 has 20 Address Outputs; 62864 has 16 Address Inputs*

8088 Memory Map Example

(8-bit Data Bus)

- 8088 Address Range: **00000h-fffffh**
- HM62864 Address Range: **0000h – ffffh**
- Let HM62864 Occupy "Low Part" of Address Space of 8088

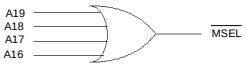
8088 Address Decoder Circuit

- "Turn On" the Memory Chip when: **A19=A18=A17=A16=0**

A19	A18	A17	A16	$\overline{MSEL}$
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

A19 A18 \ A17 A16	00	00	00	00
00	0	1	1	1
00	1	1	1	1
00	1	1	1	1
00	1	1	1	1

$\overline{MSEL} = A19 + A18 + A17 + A16$



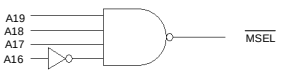
8088 Address Decoder Circuit

- "Map" HM62684 to Different Address Range: **E0000h – EFFFFh**
- Need $\overline{CS2}$=0 when: **{A19,A18,A17,A16}={1,1,1,0}**

A19	A18	A17	A16	$\overline{MSEL}$
1	1	1	0	0
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	1	1

A19 A18 \ A17 A16	00	00	00	00
00	1	1	1	1
00	1	1	1	1
00	1	1	1	0
00	1	1	1	1

$\overline{MSEL} = \overline{A19} + \overline{A18} + \overline{A17} + \overline{A16}$



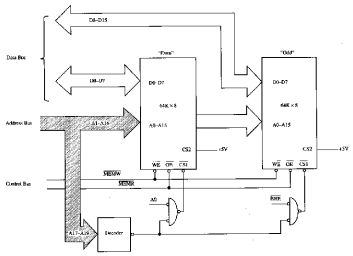
Memory Banks

- 8086/186/286/386SX has 16 Data Lines D15-D0, HM62864 Only Has 8 I/O7 – I/O0
- Must Use a "Memory Bank"
  - 1 SRAM for Storing Bytes with "Even Addresses" (… 0_2)
  - 1 SRAM for Storing Bytes with "Odd" Addresses" (… 1_2)
- 8086 has BHE Control Signal – (Bank High Enable)
- Can Use Combination of A0 and BHE to Determine Type of Access

BHE	A0	Access Type
0	0	1 word (16-bits)
0	1	Odd Byte (D15-D8)
1	0	Even Byte (D7-D0)
1	1	No Access

86,186,286,386SX Memory Interface

- Connect CPU A16-A1 Outputs to Memory Chip A15-A0 Inputs
- Use A0 and $\overline{BHE}$ to "Select" the Correct Memory Chip
- "Bank Select" Circuit



Misaligned Access

- 1 Word = 16 bits – Can Have a Misaligned Access

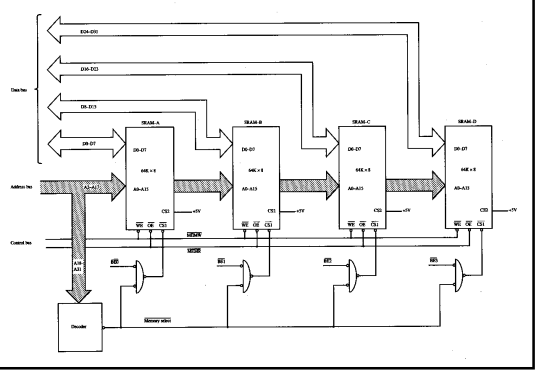
MSB	LSB	Access
odd	*even*	*aligned*
even	*odd*	*misaligned*

- Misaligned Words Require 2 Bus Cycles! (2)(2.3T)=4.6T
  1) Access LSB (odd) Byte on D15-D8
  2) Access MSB (even) Byte on D7-D0
- "Aligning" Program Data Can Speed Up Execution
  - "Wastes" Memory (fragments RAM)
  - Most Optimizing Compilers do it Automatically
  - Up to Assembler Language Programmer

80386DX and 80486 Memory Interface
(32 bit)

- 4 Banks of Byte-Wide RAM Required
- With HM62864 – Minimum Memory Size is 256kB
  - need 4 of these 64k×8 Chips
- These Processors are Restricted to Aligned Access
  - Do Not Have A1, A0 Pins
  - Do Have $\overline{BE3}$, $\overline{BE2}$, $\overline{BE1}$, $\overline{BE0}$ (*Byte Enables*)
- Memory Bank is Selected Using the Byte Enable Signals

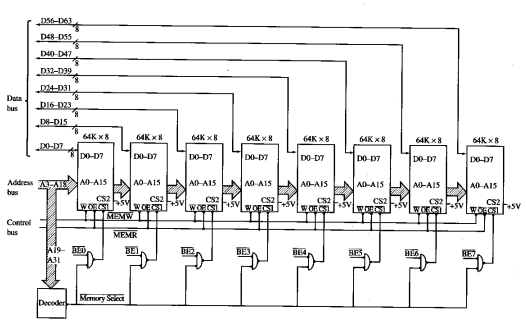
80386DX/80486 with 256kB Memory



Pentium+ Memory Interface
(64 bit)

- 8 Banks of Byte-Wide RAM Required
- With HM62864 – Minimum Memory Size is512kB
  - need 8 of these 64k×8 Chips
  - at least 1 chip per bank (byte)
- These Processors are Restricted to Aligned Access
  - Do Not Have A2, A1, A0 Pins
  - Do Have $\overline{BE7}$ - $\overline{BE0}$ (*Byte Enables*)
- Memory Bank is Selected Using the Byte Enable Signals

Pentium+ with 512kB Memory



Address Decoding

- General
  1) MS Address Lines Used as Decoder Inputs
  2) LS Address Lines Used to Select Memory Banks
  3) "Middle Address Lines" Connected Directly to Memory Chip Address Inputs
- Address Decoder
  - Circuit with MS Address Lines as Inputs
  - Output is the Chip Select (CS) Signal(s)
- Address Decoder Logic "Decides" Where Memory is Located
  - Memory Map

Book Reviews Logic Design – PALs, CUPL, etc. – Read This On Your Own

XT Memory Map