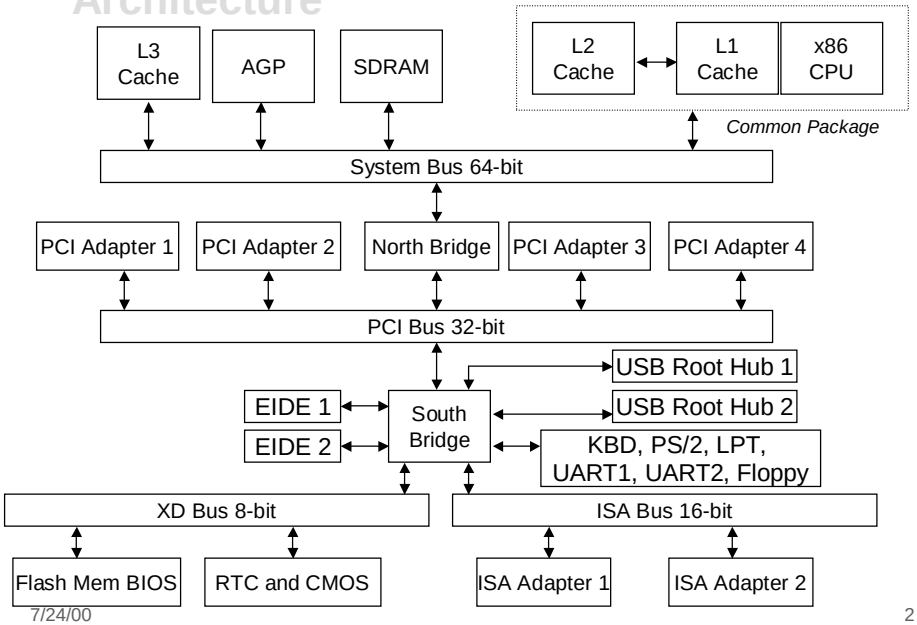
Motherboard Chipsets

- Provided by CPU manufacturer (Intel, AMD, etc)
- Provide integration of several common functions
  - Cache Controller
  - PCI Bus Interface
  - Dram Controller
  - Bridges to other busses
    - ISA, USB, etc.
- Used to be provided by third party vendors but these could not keep up with complexity of new CPUs, also hard to make time to market goals.

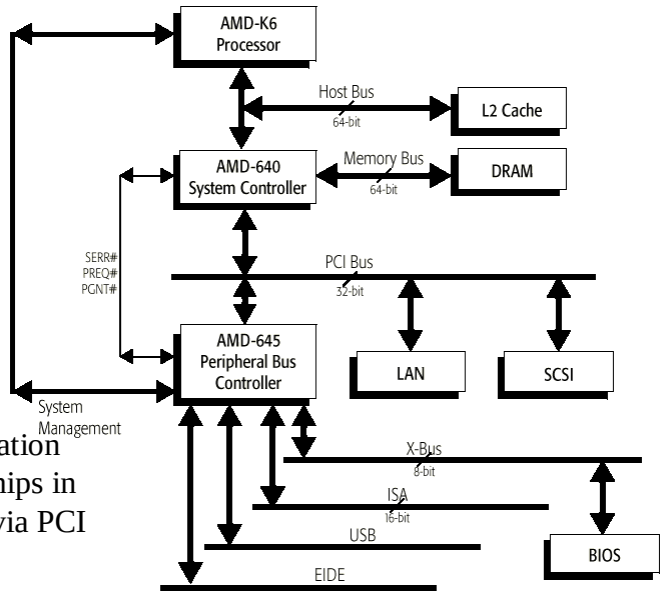
7/24/00 1

Typical PCI Based x86 Computer Architecture



7/24/00 2

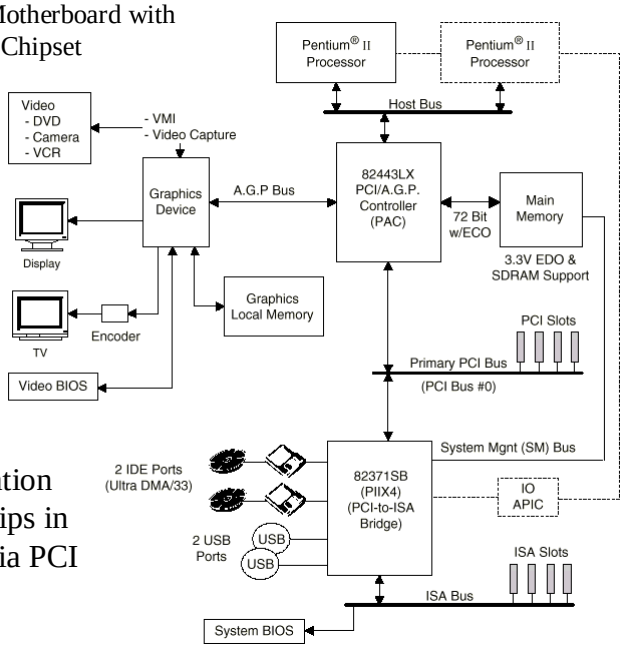
AMD Motherboard



Note that communication between chips in chipset is via PCI bus

7/24/00 3

Pentium II Motherboard with Intel 440LX Chipset



Note that communication between chips in chipset is via PCI bus

7/24/00 4

INTEL 440LX AGPSET: 82443LX PCI A.G.P. CONTROLLER (PAC)

- Supports the Pentium® II Processor at a Bus Frequency of 66 MHz
  - Supports 32-Bit Addressing
  - Optimized In-Order and Request Queue
  - Full Symmetric Multi-Processor (SMP) Protocol for Up to Two Processors
  - Dynamic Deferred Transaction Support
  - GTL+ Compliant Host Bus Supports WC Cycles
- Integrated DRAM Controller
  - EDO (Extended Data Out), and Synchronous DRAM Support
  - Supports a Maximum Memory Size of 512 MB With SDRAM, or 1 GB With EDO
  - 64/72-bit Path to Memory
  - Configurable DRAM Interface
  - Support for Auto Detection of Memory Type: (DIMM Serial Presence Detect)
  - 8 RAS Lines Available
  - Support for 4-, 16- and 64-Mbit DRAM devices
  - Support for Symmetrical and Asymmetrical DRAM Addressing
  - Configurable Support for ECC/EC
  - ECC With Single Bit Error Correction and Multiple Bit Error Detection
  - Read-Around-Write Support for Host and PCI DRAM Read Accesses
  - Supports 3.3V DRAMs
- Accelerated Graphics Port (A.G.P.) Interface
  - A.G.P. Specification Compliant
  - A.G.P. 66/133 MHz 3.3V Devices Supported
  - Synchronous Coupling to the Host Bus Frequency
- PCI Bus Interface
  - PCI Revision 2.1 Interface Compliant
  - Greater Than 100-MBps Data Streaming for PCI-to-DRAM Accesses
  - Integrated Arbiter With Multi-Transaction PCI Arbitration Acceleration Hooks
  - Five PCI Bus Masters are Supported in Addition to the Host and PCI-to-ISA I/O Bridge
  - Delayed Transaction Support
  - PCI Parity Checking and Generation Support
- Data Buffering For Increased Performance
  - Extensive CPU-to-DRAM, PCI-to-DRAM, and A.G.P.-to-DRAM Write Data Buffering
  - CPU-to-A.G.P., PCI-to-A.G.P., and A.G.P.-to-PCI Data Buffering
  - Write Combining Support for CPU-to-PCI Burst Writes
  - Supports Concurrent Host, PCI, and A.G.P. Transactions to Main Memory
- System Management Mode (SMM) Compliant
- 492 Pin BGA Package

7/24/00 5

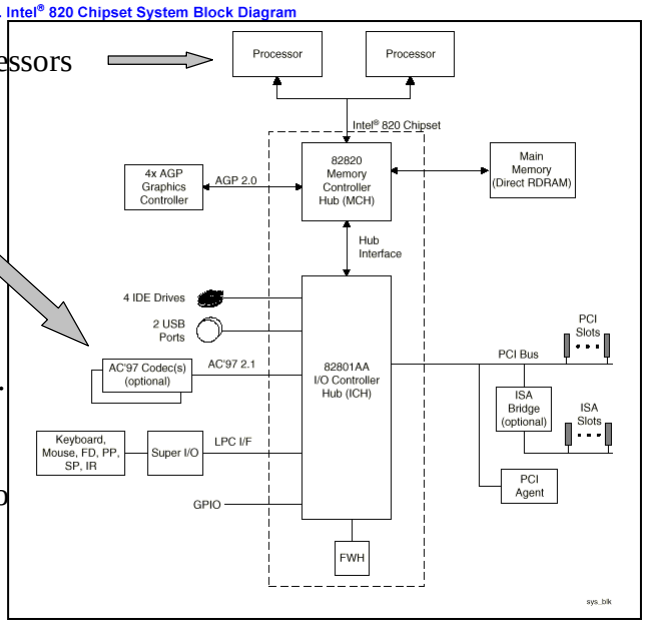
INTEL 820 Chipset (for Pentium III)

82801AA ICH functions and capabilities include:

- PCI Rev 2.2 compliant with support for 33 MHz PCI operations
- Supports up to 6 Req/Gnt pairs (PCI Slots)
- Power Management Logic Support
- Enhanced DMA Controller, Interrupt Controller and Timer Functions
- Integrated IDE controller; Ultra ATA/66
- USB host interface with support for 2 USB ports
- System Management Bus (SMBus) compatible with most I^2C devices
- AC'97 2.1 Compliant Link for Audio and Telephony CODECs
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Alert on LAN*

7/24/00 6

Figure 1. Intel® 820 Chipset System Block Diagram



Two processors supported

Winmodem support

"Hub" architecture. Dedicated comm link between two chips of chipset

I82802 Firmware Hub

- Optional component for all 810 and above chipsets
- 4 or 8 Mbits of flash memory for non-volatile storage (can be used by BIOS)
- Contains a Random number generator based on thermal noise
  - Actual RNG instead of psuedo-RNG can increase security of encryption algorithms

Low Pin Count (LPC) interface

- Intended to be new interface between legacy devices (ISA, X-bus) and chipset
- Devices that interface with chipset thru LPC interface:
  - SuperIO devices (Keyboard, Serial Port, parallel port, Floppy Disk Controller)
  - Generic memory (BIOS)
- Uses PCI 33 Mhz clock
- Goal is a PC without either X-Bus or ISA

7/24/00 9

Intel 815E Chipset

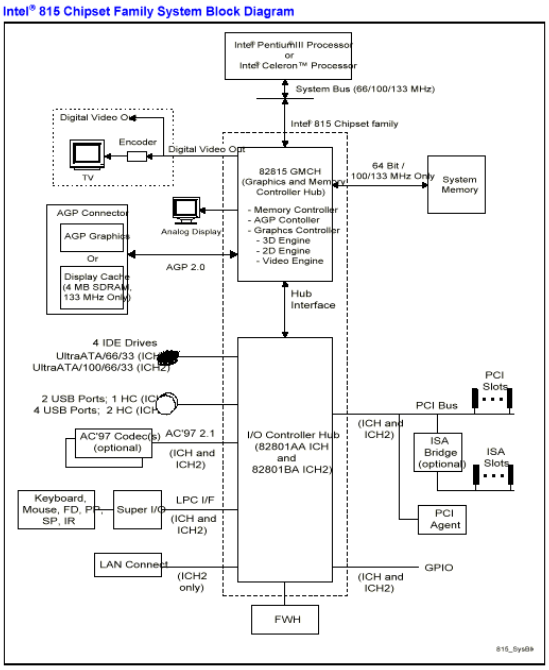
- Intended for low cost to midstream PCs
- 3D graphics controller (low-performance, based on i740 3D graphics chip) integrated on chipset!
- SDRAM controller
- 2 USB controllers
- AGP port also included – if on-chip 3D controller is used, then AGP port used for texture cache
- LAN controller integrated (10/100 Mbit ethernet)
- All of the other usual stuff

7/24/00 10

815E block diagram

AGP port can support an external 3D video card

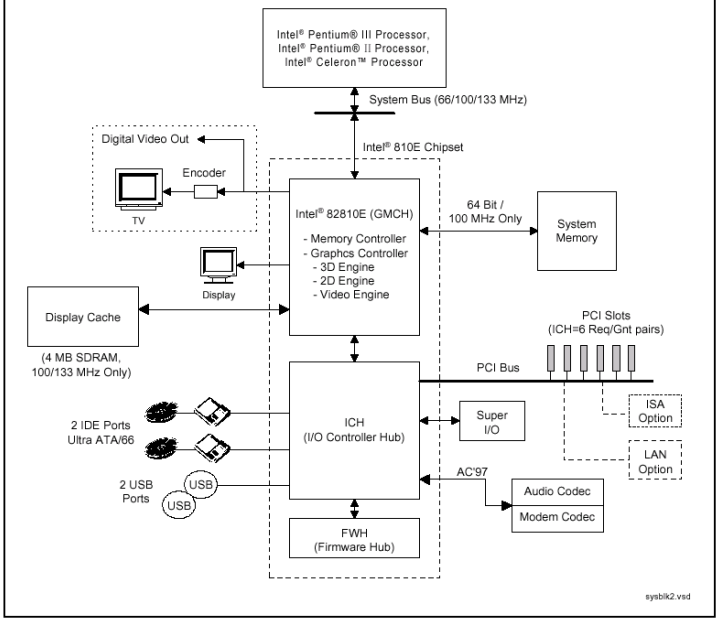
Figure 1. Intel® 815 Chipset Family System Block Diagram



810 Chipset, cheaper version of 815.

No AGP port, intended for low cost PCs.

Figure 1. Intel® 810E Chipset System Block Diagram With Intel 82810E GMCH and ICH



AGP - Advanced Graphics Port

- A dedicated, bi-directional, point-to-point bus meant for high speed transfers between the graphics adapter and system memory
- Major problem with graphics card is memory
  - Often need a lot of it (> 8Mb)
  - If this memory is placed on graphics card, then card is expensive.
  - If System memory is used, then access over PCI bus is slow
    - Solution, Add new dedicated bus!!!

7/24/00 13

AGP Data Paths

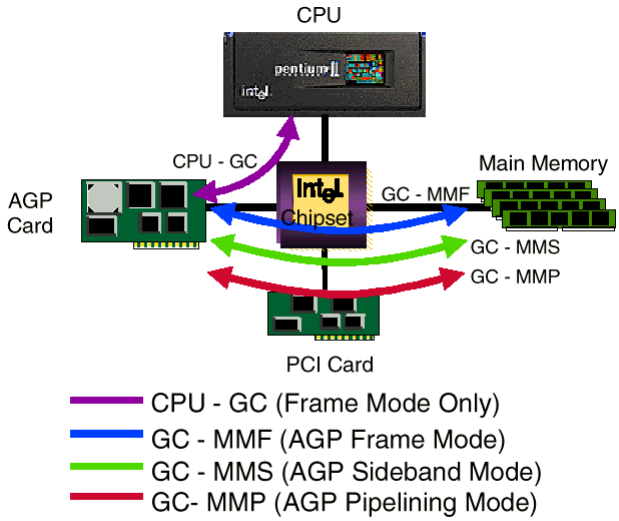
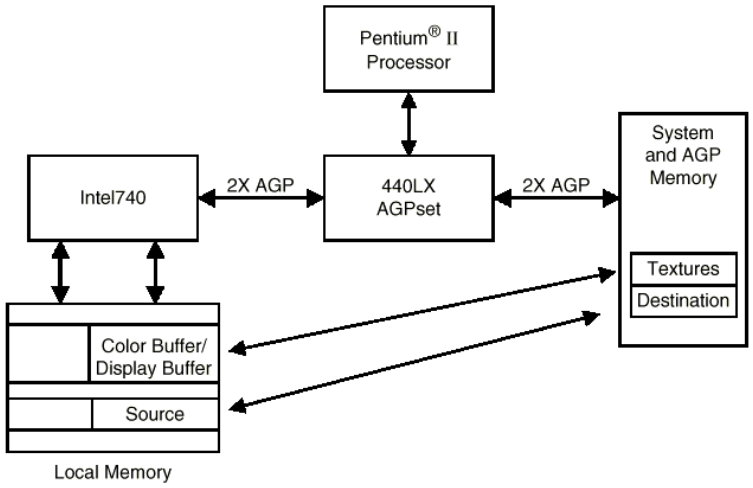


Figure 1: Data Movement Paths and Corresponding AGP Modes.

7/24/00 14

Intel 740 3D Graphics Controller and AGP



7/24/00 15

Key Features of AGP

- Allows dual edge clocking on 66 Mhz bus
  - Data transferred on BOTH edges of clock (called 2X AGP)
  - Data bandwidth is 4 bytes * 133 Mhz = 533 MB/s
  - AGP 2.0 added 4X mode to increase bandwidth to 1066 MBs
- Implements sideband addressing for transaction commands
  - Separate command bus for transaction commands
  - Can queue up multiple transactions via command bus, data transfer on data bus is continuous as one transaction finishes and another begins.

7/24/00 16

Effect of Sideband Command Capability

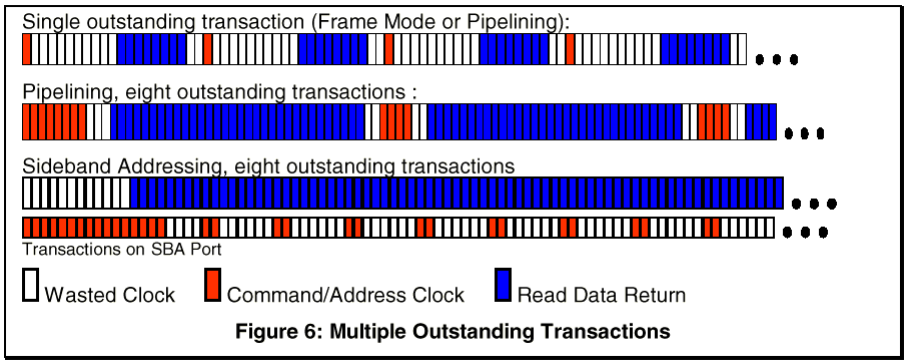


Figure 6: Multiple Outstanding Transactions

SBA port is a seperate port (8 bits) that contains just command data. Does not have to be used, main data bus can be used to pass all commands/data/addresses.

7/24/00 17

AGP 2X Transfer -- AD_STBx is driven by chipset

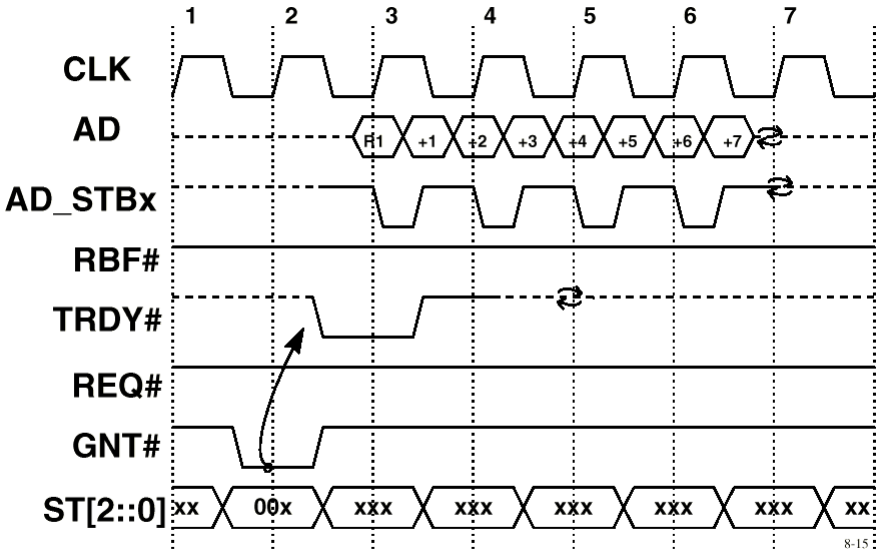


Figure 3-25: 2x Read Data - No Delay

8

AGP 4X Transfer

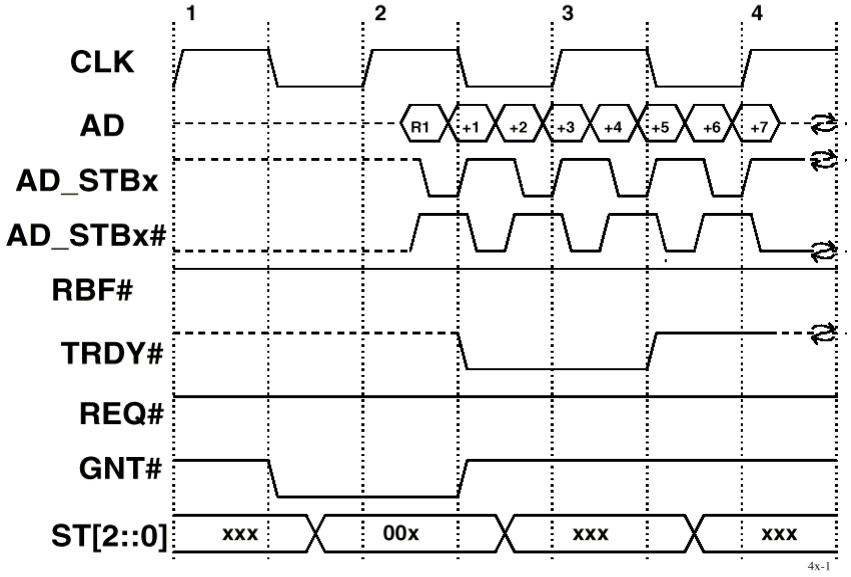


Figure 3-31: 4x Read Data - No Delay

Characteristics of High Performance Busses

- Wider is better (at least 32-bit data width)
- Dual edge clocking
- Split Transactions (issue a command to IO device to start transfer), then come back later when data is ready
- Bus Mastership
- Advanced Signaling
  - Limited voltage swing, differential signaling

7/24/00 20

Pentium II/III GTL Bus (Host Bus)

- Gunning Transceiver Logic (GTL) used for Pentium II local bus (66Mhz now, 100Mhz, 133 Mhz)
  - GTL bus is open drain bus where all runs are terminated
  - Termination voltage (Vtt) is 1.5 v.
- GTL bus is a differential bus with only wire!
  - Vref used by all receivers, drivers
    - Vref (1.0v) is 2/3 of Vtt .
  - Voltage swing about Vref is +/- 200 mv.
    - Less voltage swing => higher speed, less noise margin

7/24/00 21

GTL Bus (continued)

- Interconnections on a GTL bus are transmission lines so interconnect topology, termination very important.
- Interconnection is point to point to avoid stubs (stubs generate reflections)

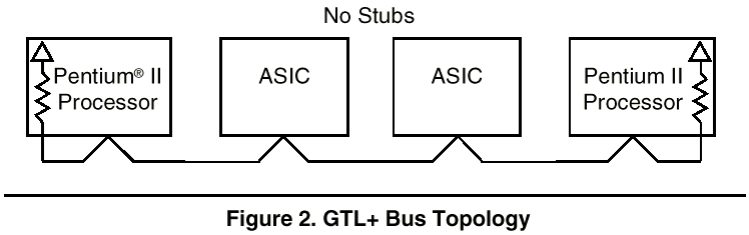


Figure 2. GTL+ Bus Topology

7/24/00 22