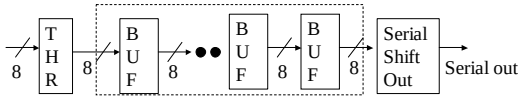
16550D UART (Section 10.3)

- UART – Universal Asynchronous Receiver/Transmitter
  - support chip for serial I/O in x86 architectures
- Original device was 16550, the 16550D contains two 16550s ('D' stands for Dual)
- Function is send and receive data via the asynchronous serial protocol discussed in the previous lecture
- Figure 10-19 in textbook shows register set

Register Set (Data)

- 8 registers total
  - On PC, one set mapped to ports 3F8-3FF (COM1), other set mapped to 2F8-2FF (COM2)
- Data registers (all 8 bits) (See Table 10.6)
  - Receive buffer register (RBR) – holds incoming serial data (offset 0, read only)
  - Transmit holding register (THR) holds outgoing serial data (offset 0, write only, name: THR)
  - Scratch register (offset 7) – used to hold temporary data
- Receive/Transmit Data registers have FIFO's in front of them for more efficient operation.

FIFO – First In First Out Buffer

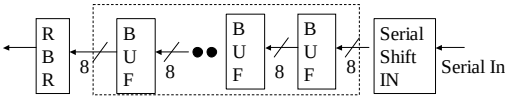


16 byte FIFO

Advantage of a FIFO on output of THR is that don't have to wait for serial shift out to finish before we send more data to THR. The THR contents immediately sent to FIFO. Only have to wait if FIFO becomes full.

If FIFO is not enabled, then after writing byte to THR, have to wait until it is shifted out the serial line.

FIFO on RBR (Receive Buffer Register)



16 byte FIFO

When 8 bits of serial data arrived, immediately sent to RBR via FIFO. While waiting for processor to empty the RBR by reading it, additional serial data can arrive and is stored in the FIFO. Processor HAS to read the RBR before the FIFO becomes entirely full or data will be lost.

Control Registers

- Interrupt Enable Register (IER, offset 1) – used to enable to interrupts on various conditions
  - Data available interrupt
  - Transmitter Data Register empty
- FIFO Control Register (FCR, offset 2, write only)
  - Used to configure FIFO operation
- Line Control Register (LCF, offset 3)
  - sets data format for serial transfer
- Modem Control Register (MCR, offset 4)
  - controls modem output handshaking lines

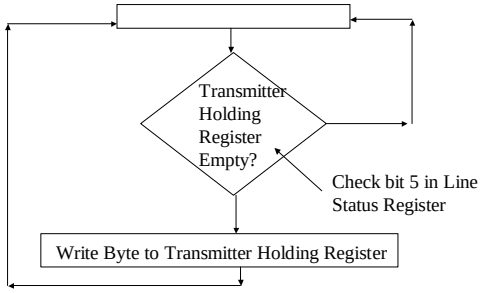
Status Registers

- Interrupt Identification Register (IIR, offset 2, read only)
  - Used to identify source of an interrupt
- Line Status Register (LSR, offset 5)
  - status bits to determine when data is received, data has been sent, various error conditions
- Modem Status Register (MSR)
  - Use to control output handshaking signals for modem interface.

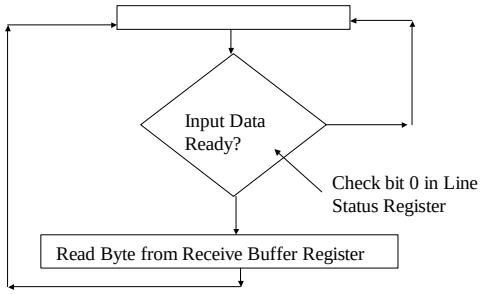
Port Mapping

RBR (read only)	3F8	2F8
THR (write only)	3F8	2F8
IER	3F9	2F9
IIR (read only)	3FA	2FA
FCR (write only)	3FA	2FA
LCR	3FB	2FB
MCR	3FC	2FC
LSR	3FD	2FD
MSR	3FE	2FE
SCR	3FF	2FF

Send A Byte (Polled I/O)



Receive A Byte (Polled I/O)



Error Conditions

- Overrun Error (Bit 1 in Line Status Register)
  - Did not read Receive Data Register fast enough. Incoming data overwrote current data
- Parity Error (Bit 2 in Line Status Register)
  - Incoming data had incorrect parity
- Framing Error (Bit 3 in Line Status Register)
  - Invalid stop bit received (received too soon or too late)

Interrupt Conditions

- Use the IER (Interrupt Enable Register) to enable interrupt conditions
  - Bit 0 enables Received Data Interrupt (generate interrupt when data is received)
  - Bit 1 enables Transmitter Holding Register Empty Interrupt (interrupt when data is finished being sent)
- Use the IIR (Interrupt Identification Register) to determine what caused an interrupt
  - Bit 0 is for received data interrupt
  - Bit1 is for THRE interrupt

Interrupts and the FIFOs

- Receive Buffer FIFO
  - Can program the receive buffer FIFO to generate an interrupt when FIFO has either 1, 4, 8 or 14 bytes in it.
  - Bits 7,6 of the FIFO Control register control this setting
- Transmit Buffer FIFO
  - if Transmit interrupts are enabled and FIFO is enabled, then will only generate an interrupt when the transmit buffer FIFO is empty.

Setting Data Format, Baud Rate

- Line Control Register used to set data format
  - number of data bits (5,6,7, or 8)
  - number of stop bits (1 or 2)
  - Parity on (even or odd), or Off
- To set baud rate, need to set Bit 7 of LCR to a '1'
  - This bit is called the 'Divisor Latch Access Bit' and changes registers 0,1 to be the low, high 'divider' configuration registers
  - Programming registers low,high divider register will set a divide-by rate of the input clock setting a clock speed (table 10.8).
  - After setting speed, Bit 7 of LCR needs to be set back to 0 for normal operation.