RAMBUS® DRAM

MT6V8M16 - 256K x 16 x 32 banks
MT6V8M18 - 256K x 18 x 32 banks

For the latest data sheet, please refer to the Micron Web site:
www.micron.com/mti/msp/html/datasheet.html

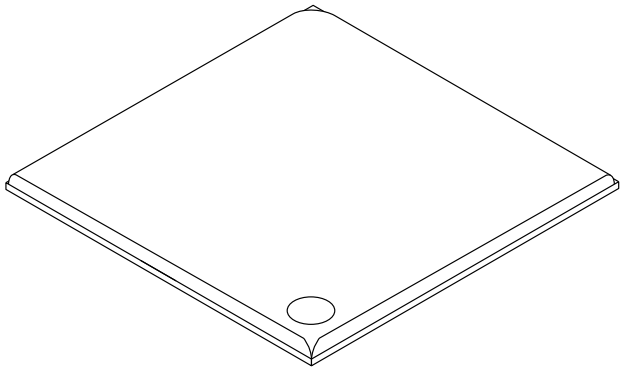
FEATURES

- High-speed 300 MHz, 356 MHz, and 400 MHz clocks with 2x data rates
- 1.6 GB/s peak I/O bandwidth at the 400 MHz clock
- Rambus® signaling level (RSL) using differential 300 MHz, 356 MHz, and 400 MHz transmit and receive clocks
- Packet-oriented Rambus protocol transmitted in 8-bit-long packets
- Separate control (8-bit) and data (18-bit) buses for increased data bandwidth capability
- Control bus with separate row (3-bit) and column (5-bit) buses for easier command scheduling
- Programmable output delay timing for roundtrip delay of one to five cycles
- Support for up to four simultaneous transactions (within bank restrictions)
- Write buffer to reduce READ latency
- Three precharge mechanisms for controller flexibility
- Programmable power states for flexibility in power consumption versus data access time
- Power-down Self-Refresh and Active Refresh
- Organization: 1KB pages and 32 banks, x16 or x18
- FBGA package in standard and mirrored pinout
- 32ms, 16,384 cycle refresh
- 2.5V power supply with 1.8V CMOS supply for I/Os

OPTIONS — NUMBER

- Configurations
  - 8 Meg x 16 — 8M16
  - 8 Meg x 18 — 8M18
- Package/Pinout
  - FBGA (standard pinout, 54-pin, 4-row depop) — F
  - FBGA (standard pinout, 62-pin, 2-row depop) — F1
  - FBGA (mirrored pinout, 62-pin, 2-row depop) — R1
- Timing (Cycle Time)
  - 300 MHz Clock Rate, Access Time = 53ns — -3M
  - 356 MHz Clock Rate, Access Time = 50ns — -3B
  - 356 MHz Clock Rate, Access Time = 45ns — -3C
  - 400 MHz Clock Rate, Access Time = 45ns — -4C

FBGA
(Top View)



RDRAM® PART NUMBERS

(shown for standard pinout 2-row depopulated FBGA package)

PART NUMBER	ORGANIZATION[1]	CLK FREQ. (MHz)	ACCESS TIME (ns)
MT6V8M16F1-3M	256K x 16 x 32	300	53
MT6V8M16F1-3B	256K x 16 x 32	356	50
MT6V8M16F1-3C	256K x 16 x 32	356	45
MT6V8M16F1-4C	256K x 16 x 32	400	45
MT6V8M18F1-3M	256K x 18 x 32	300	53
MT6V8M18F1-3B	256K x 18 x 32	356	50
MT6V8M18F1-3C	256K x 18 x 32	356	45
MT6V8M18F1-4C	256K x 18 x 32	400	45

NOTE: 1. The "32" designation indicates that this RDRAM core is comprised of 32 banks which use a "split" bank architecture.

GENERAL DESCRIPTION

The MT6V8M16 RDRAM® is a general-purpose, high-performance, packet-oriented, dynamic random-access memory containing 134,217,728 bits. The MT6V8M16 is internally configured as 32 banks of 32K x 128; each of the 32K x 128 banks is organized as 512 rows by 64 columns by 128 bits. The 128 bits are serially multiplexed onto the RDRAM's I/O pins as eight 16-bit words.

The MT6V8M18 RDRAM is a general-purpose, high-performance, packet-oriented, dynamic random-access memory containing 150,994,944 bits. The MT6V8M18 is internally configured as 32 banks of 32K x 144; each of the 32K x 144 banks is organized as 512 rows by 64 columns by 144 bits. The 144 bits are serially multiplexed onto the RDRAM's I/O pins as eight 18-bit words.

The MT6V8M16/MT6V8M18 use Rambus signaling level (RSL) technology to achieve 356 MHz or 400 MHz clock speeds using differential clocks. Control and I/O data is transferred on both rising and falling edges of the clock. This allows data transfers at 1.25ns per two bytes (10ns per 16 bytes) during peak operation.

All DRAM commands are communicated to the MT6V8M16/MT6V8M18 through a 3-bit row or 5-bit column bus in packets which are 8 bits in length. These packets are then decoded on the RDRAM into the operation and address requiring access.

Initialization and mode configuration for the MT6V8M16/MT6V8M18 are accessed through the slow-speed CMOS serial I/O interface.

The architecture of RDRAMs allows high sustained bandwidth memory transactions for multiple, simultaneous, semi-random addresses. The RDRAM's 32 banks can support up to four simultaneous transactions (within bank restrictions).

System-oriented features include power management, byte masking, and x18 organization. The two data bits in the x18 organization are general and can be used for additional storage and bandwidth, or for error correction.

DEVICE PINOUT

The pinout tables in Figure 1 show the pin assignments of the center-bonded RDRAM package from the top side of the package (the view looking down on the package as it is mounted on the circuit board). The MT6V8M16 and MT6V8M18 devices are available in an FBGA package. Both devices are offered in 54-pin standard-pinout package with four rows of balls depopulated in the center of the die. This device is designated with an "F" in the part number.

The MT6V8M16 and MT6V8M18 are also available in a 62-pin FBGA package with two rows of balls depopulated. This device has eight "outrigger" balls for additional stability during reflow and improved power and ground signalling. The 62-pin FBGA is available in a standard pinout designated with an "F1" in the part number. It is also available in a mirrored pinout designated as "R1" for improved routing on applications requiring mounting the RDRAMs on both sides of the printed circuit board.

FBGA Package Pinouts

Standard Pinout "F" 4-Row Depopulated (Top View)

10	DQA7	DQA4	CFM	CFMN	RQ5	RQ3	DQB0	DQB4	DQB7
9	GND	V_{DD}	GND	GNDa	V_{DD}	GND	V_{DD}	V_{DD}	GND
8	CMD	DQA5	DQA2	$V_{DD}a$	RQ6	RQ2	DQB1	DQB5	SIO1
7									
6									
5									
4									
3	SCK	DQA6	DQA1	V_{REF}	RQ7	RQ1	DQB2	DQB6	SIO0
2	V_{CMOS}	GND	V_{DD}	GND	GND	V_{DD}	GND	GND	V_{CMOS}
1	DQA8	DQA3	DQA0	CTMN	CTM	RQ4	RQ0	DQB3	DQB8
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**

Standard Pinout "F1" 2-Row Depopulated (Top View)

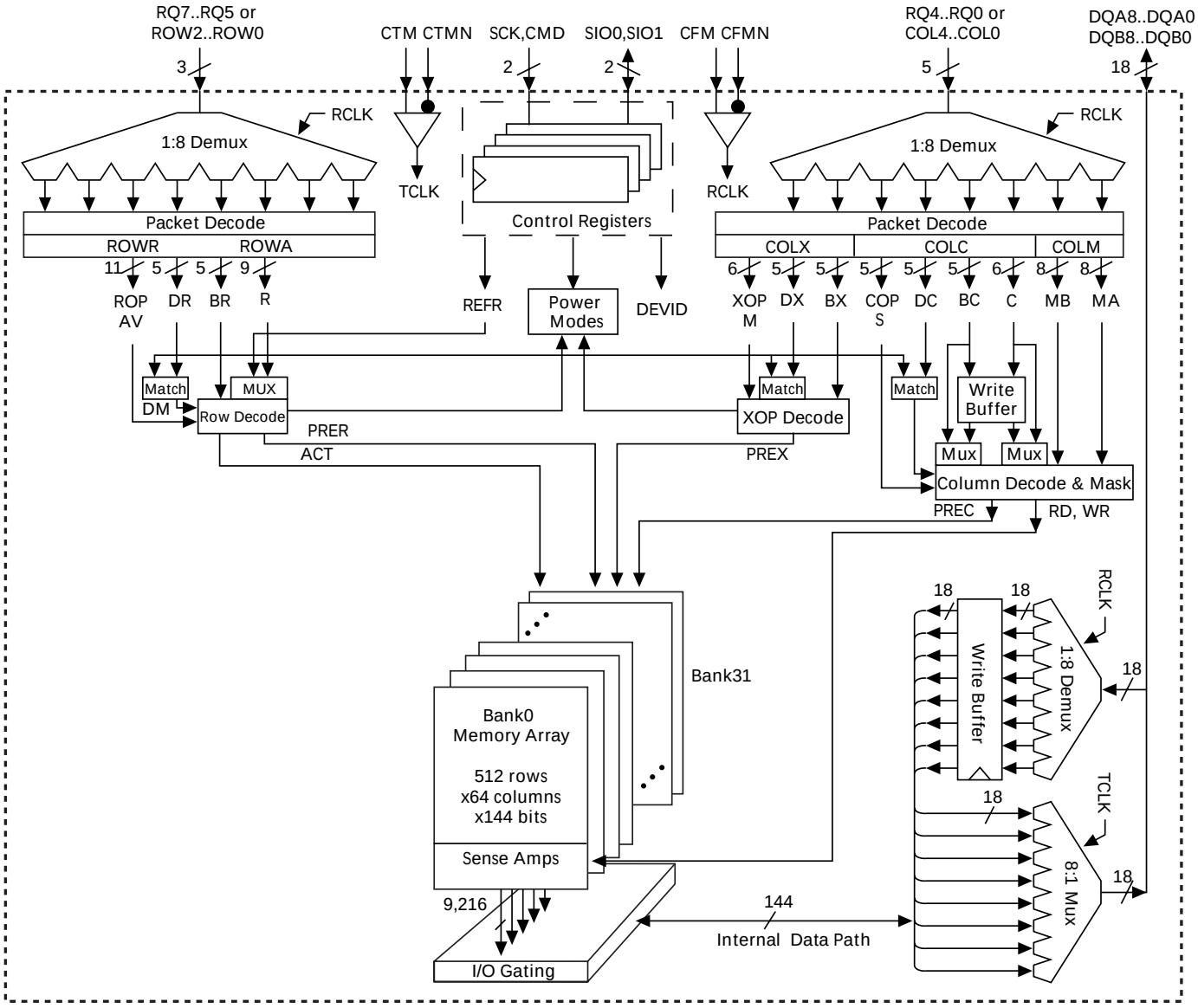
12	GND		V_{DD}				V_{DD}		GND
11									
10	DQA7	DQA4	CFM	CFMN	RQ5	RQ3	DQB0	DQB4	DQB7
9	GND	V_{DD}	GND	GNDa	V_{DD}	GND	V_{DD}	V_{DD}	GND
8	CMD	DQA5	DQA2	$V_{DD}a$	RQ6	RQ2	DQB1	DQB5	SIO1
7									
6									
5	SCK	DQA6	DQA1	V_{REF}	RQ7	RQ1	DQB2	DQB6	SIO0
4	V_{CMOS}	GND	V_{DD}	GND	GND	V_{DD}	GND	GND	V_{CMOS}
3	DQA8	DQA3	DQA0	CTMN	CTM	RQ4	RQ0	DQB3	DQB8
2									
1	GND		V_{DD}				V_{DD}		GND
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**

Mirrored Pinout "R1" 2-Row Depopulated (Top View)

12	GND		V_{DD}				V_{DD}		GND
11									
10	DQA8	DQA3	DQA0	CTMN	CTM	RQ4	RQ0	DQB3	DQB8
9	V_{CMOS}	GND	V_{DD}	GND	GND	V_{DD}	GND	GND	V_{CMOS}
8	SCK	DQA6	DQA1	V_{REF}	RQ7	RQ1	DQB2	DQB6	SIO0
7									
6									
5	CMD	DQA5	DQA2	$V_{DD}a$	RQ6	RQ2	DQB1	DQB5	SIO1
4	GND	V_{DD}	GND	GNDa	V_{DD}	GND	V_{DD}	V_{DD}	GND
3	DQA7	DQA4	CFM	CFMN	RQ5	RQ3	DQB0	DQB4	DQB7
2									
1	GND		V_{DD}				V_{DD}		GND
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**

NOTE: For the MT6V8M16 device, DQA8 and DQB8 are no connects.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The drawing is for the MT6V8M18 device. The MT6V8M16 device has a 128-bit internal bus width (instead of 144) and DQA8/DQB8 are not used.

DEVICE MARKING

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. (See Fig. 1.) The abbreviated device marks are cross referenced to Micron part numbers in Table 1.

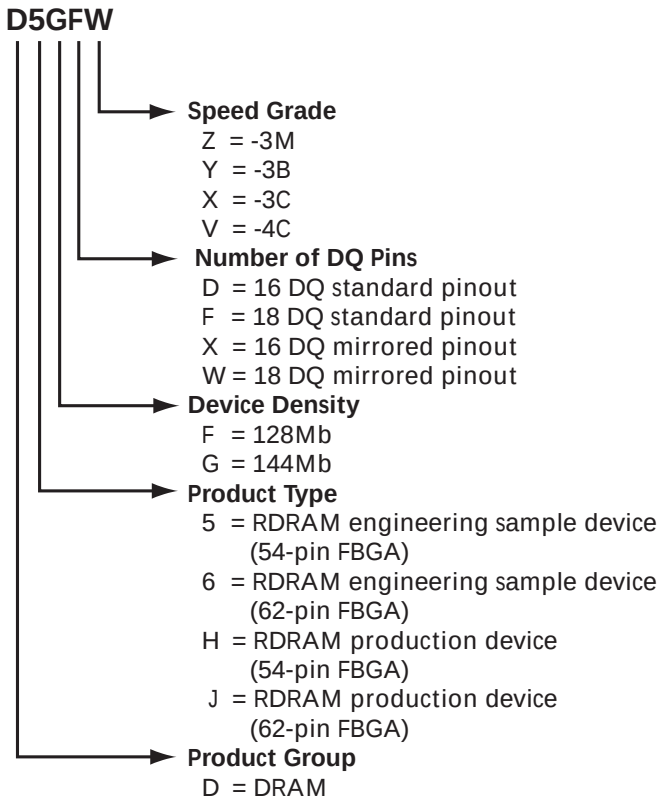


Figure 1
Abbreviated Device Mark

Table 1
Cross Reference for Abbreviated Device Marks

(62-pin Depop Shown)

			54-PIN "F" FBGA		62-PIN "F1" FBGA		62-PIN "R1" FBGA	
PART NUMBER	CLK FREQ. (MHz)	ACCESS TIME (ns)	SAMPLE MARKING	PRODUCT MARKING	SAMPLE MARKING	PRODUCT MARKING	SAMPLE MARKING	PRODUCT MARKING
MT6V8M16F-3M	300	53	D5FDZ	DHFDZ	D6FDZ	DJFDZ	D6FXZ	DJFXZ
MT6V8M16F-3B	356	50	D5FDY	DHFDY	D6FDY	DJFDY	D6FXY	DJFXY
MT6V8M16F-3C	356	45	D5FDX	DHFDX	D6FDX	DJFDX	D6FXX	DJFXX
MT6V8M16F-4C	400	45	D5FDV	DHFDV	D6FDV	DJFDV	D6FXV	DJFXV
MT6V8M18F-3M	300	53	D5GFZ	DHGFZ	D6GFZ	DJGFZ	D6GWZ	DJGWZ
MT6V8M18F-3B	356	50	D5GFY	DHGFY	D6GFY	DHGFY	D6GWY	DJGWY
MT6V8M18F-3C	356	45	D5GFX	DHGFX	D6GFX	DJGFX	D6GWX	DJGWX
MT6V8M18F-4C	400	45	D5GFV	DHGFV	D6GFV	DJGFV	D6GWV	DJGWV

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