MICRON SEMICONDUCTOR PRODUCTS, INC.

512K x 18
2.5V VDD, HSTL, QDRb2 SRAM

9Mb QDR™ SRAM 2-Word Burst

MT54V512H18A

FEATURES

- 9Mb Density (512K x 18)
- Separate independent read and write data ports with concurrent transactions
- 100% bus utilization DDR READ and WRITE operation
- High frequency operation with future migration to higher clock frequencies
- Fast clock to valid data times
- Full data coherency, providing most current data
- Two-tick burst counter for low DDR transaction size
- Double data rate operation on read and write ports
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two output clocks (C and C#) for precise flight time and clock skew matching—clock and data delivered together to receiving device
- Single address bus
- Simple control logic for easy depth expansion
- Internally self-timed, registered writes
- +2.5V core and HSTL I/O
- Clock-stop capability
- 13x15mm, 1mm pitch, 11 x 15 grid FBGA package
- User programmable impedence output
- JTAG boundary scan

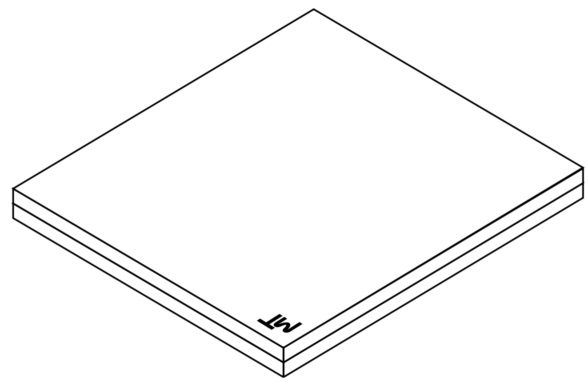
OPTIONS / MARKING

OPTIONS	MARKING
• Clock Cycle Timing	
6ns (167 MHz)	-6
7.5ns (133 MHz)	-7.5
10ns (100 MHz)	-10
• Configuration	
512K x 18	MT54V512H18A
• Package	
165-pin, 13mm x 15mm FBGA	F

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT54V512H18AF-xx	512K x 18, QDRb2 FBGA

165-Pin FBGA



GENERAL DESCRIPTION

The Micron® QDR™ (Quad Data Rate™) Synchronous Pipelined Burst SRAM employs high-speed, low-power CMOS designs using an advanced 6T CMOS process. The QDR architecture consists of two separate DDR (double data rate) ports to access the memory array. The read port has dedicated data outputs to support READ operations. The write port has dedicated data inputs to support WRITE operations. This architecture eliminates the need for high-speed bus turnaround. Access to each port is accomplished using a common address bus. Addresses for reads and writes are latched on rising edges of the K and K# input clocks, respectively. Each address location is associated with two 18-bit words that burst sequentially into or out of the device. Since data can be transferred into *and* out of the device on every rising edge of both clocks (K, K#, C and C#) memory bandwidth is maximized while simplifying system design by eliminating bus turnarounds.

Depth expansion is accomplished with port selects for each port (read R#, write W#) which are received at K rising edge. Port selects permit independent port operation. All synchronous inputs pass through registers controlled by the K or K# input clock rising edges. Active LOW byte writes (BW0#, BW1#) permit byte write selection. Write data and byte writes are registered on the rising edges of both K and K#. The addressing within each burst of two is fixed and sequential, beginning with the lowest and ending with

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GENERAL DESCRIPTION (continued)

the highest address. All synchronous data outputs pass through output registers controlled by the rising edges of the output clocks (C and C# if provided, otherwise K and K#).

Four pins are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK) and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use JEDEC-standard 2.5V I/O levels to shift data during this testing mode of operation.

The SRAM operates from a +2.5V power supply, and all inputs and outputs are HSTL-compatible. The device is ideally suited for applications that benefit from a high-speed fully-utilized DDR data bus.

Please refer to Micron's Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest data sheet.

READ/WRITE OPERATIONS

All bus transactions operate on an uninterruptable burst of two data, requiring one full clock cycle of bus utilization.The resulting benefit is that short data transactions can remain in operation on both buses provided that the address rate can be maintained by the system (2x the clock frequency).

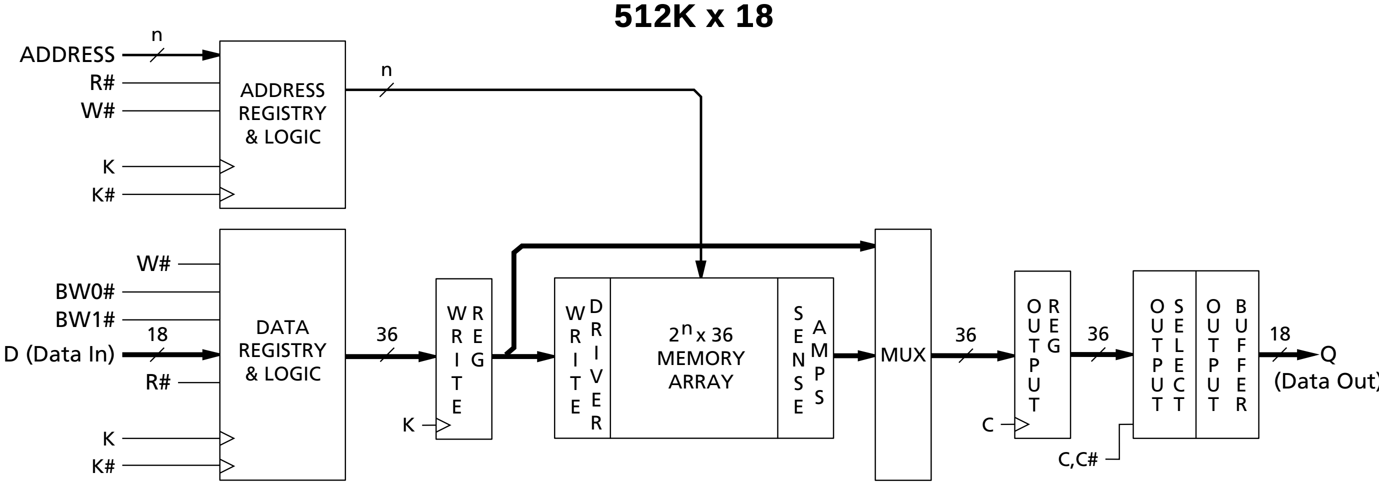
READ cycles are pipelined. The request is initiated by asserting R# LOW at K rising edge. Data is delivered after the next rising edge of K using C and C# as the output timing references, or using K and K# if C and C# are tied HIGH. If C and C# are tied HIGH, they may not be toggled during device operation. Output tri-stating is automatically controlled such that the bus is released if no data is being delivered. This permits banked SRAM systems with no complex OE timing generation. Back-to-back READ cycles are initiated every K rising edge.

WRITE cycles are initiated by W# LOW at K rising edge. The address for the WRITE cycle is provided at the following K# rising edge. Data is expected at the rising edge of K and K# beginning at the same K which initiated the cycle. Write registers are incorporated to facilitate pipelined self-timed WRITE cycles and provide fully coherent data for all combinations of READs and WRITEs. A READ can immediately follow a WRITE even if they are to the same address. Although the WRITE data has not been written to the memory array, the SRAM will deliver the data from the Write Register instead of using the older data from the memory array. The latest data is always utilized for all bus transactions. WRITE cycles can be initiated on every K rising edge.

BYTE WRITE OPERATIONS

BYTE WRITE operations are supported. The active LOW byte write controls, BW0# and BW1#, are registered coincident with their corresponding data. This feature can eliminate the need for some READ/MODIFY/WRITE cycles, collapsing it to a single BYTE WRITE operation in some instances.

FUNCTIONAL BLOCK DIAGRAM
512K x 18



NOTE: 1. The functional block diagram illustrates simplified device operation. See truth table, pin descriptions and timing diagrams for detailed information.
2. n = 18

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PROGRAMMABLE IMPEDANCE OUTPUT BUFFER

The QDR SRAM is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSS. The value of the resistor must be five times the desired impedance. For example, a 350Ω resistor is required for an output impedance of 70Ω. To ensure that output impedance is one fifth the value of RQ (within 10 percent), the range of RQ is 175Ω to 350Ω. Alternately, the ZQ pin can be connected directly to VDD, which will place the device in a minimum impedance mode.

Output impedance updates may be required because variations may occur in supply voltage and temperature over time. The device samples the value of RQ. An update of the impedance is transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set at 50Ω. To guarantee optimum output driver impedance after power-up, the SRAM needs 1,024 cycles to update the impedance. The user can operate the part with fewer than 1,024 clock cycles, but optimal output impedance is not guaranteed.

CLOCK CONSIDERATIONS

The device does not utilize internal phase-locked loops and can therefore be placed into a stopped-clock state to minimize power without lengthy restart times. It is strongly recommended that the clocks operate for a number of cycles prior to initiating commands to the SRAM. This delay permits transmission line charging effects to be overcome and allows the clock timing to be nearer to its steady-state value.

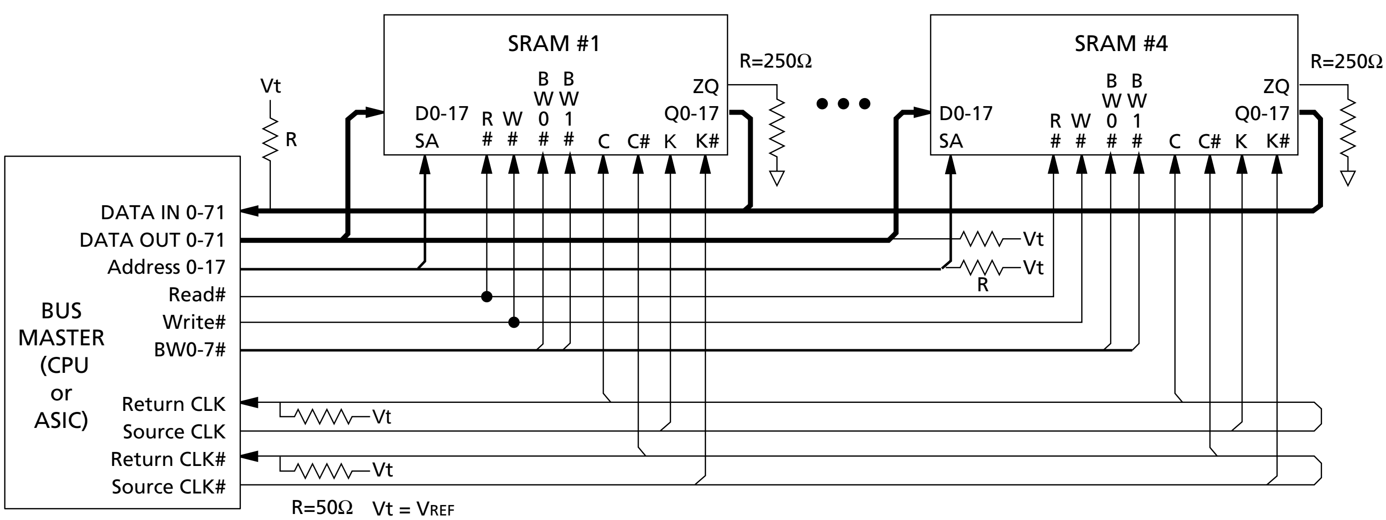
SINGLE CLOCK MODE

The SRAM can be used with the single K, K# clock pair by tying C and C# HIGH. In this mode the SRAM will use K and K# in place of C and C#. This mode provides the most rapid data output but does not compensate for system clock skew and flight times.

DEPTH EXPANSION

Port select inputs are provided for the read and write ports. This allows for easy depth expansion. Both Port Selects are sampled on the rising edge of K only. Each port can be independently selected and deselected and do not affect the operation of the opposite port. All pending transactions are completed prior to a port deselecting.

APPLICATION EXAMPLE



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PIN ASSIGNMENT (Top View)
165-Pin FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	DNU	VSS/SA*	NC/SA*	W#	BW1#	K#	NC	R#	NC/SA*	VSS/SA*	DNU
B	NC	Q9	D9	SA	NC	K	BW0#	SA	NC	NC	Q8
C	NC	NC	D10	VSS	SA	SA	SA	VSS	NC	Q7	D8
D	NC	D11	Q10	VSS	VSS	VSS	VSS	VSS	NC	NC	D7
E	NC	NC	Q11	VDDQ	VSS	VSS	VSS	VDDQ	NC	D6	Q6
F	NC	Q12	D12	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	Q5
G	NC	D13	Q13	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	D5
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	D14	VDDQ	VDD	VSS	VDD	VDDQ	NC	Q4	D4
K	NC	NC	Q14	VDDQ	VDD	VSS	VDD	VDDQ	NC	D3	Q3
L	NC	Q15	D15	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	Q2
M	NC	NC	D16	VSS	VSS	VSS	VSS	VSS	NC	Q1	D2
N	NC	D17	Q16	VSS	SA	SA	SA	VSS	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

*Expansion addresses: 9A for 18Mb, 3A for 36Mb, 10A for 72Mb, 2A for 144Mb

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PIN DESCRIPTIONS

PINS (x18)	SYMBOL	TYPE	DESCRIPTION
6C 7C 4B, 8B, 5C, 5N-7N, 4P, 5P, 7P, 8P, 3R-5R, 7R-9R	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K for READ cycles and must meet the setup and hold times around the rising edge of K# for WRITE cycles. Pins 9A, 3A, 10A, and 2A are reserved for the next higher -order address inputs on 18, 36, 72, and 144Mb devices, respectively. All transactions operate on a burst of two 18-bit data (one clock period of bus activity). These inputs are ignored when both ports are deselected.
8A	R#	Input	Synchronous Read: When LOW this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
4A	W#	Input	Synchronous Write: When LOW this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
7B 5A	BW0# BW1#	Input	Synchronous Byte Writes: When LOW these inputs cause their respective byte to be registered and written if W# had initiated a WRITE cycle. BW0# and BW1# must meet setup and hold times around the rising edges of K and K# for each of the two rising edges comprising the WRITE cycle. BW0# controls D0-D8. BW1# controls D9-D17.
6B 6A	K K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
6P 6R	C C#	Input	Output Clock: This clock pair provides a user controlled means of tuning device output data. The rising edge of C is used as the output timing reference for first output data. The rising edge of C# is used as the output reference for second output data. Ideally, C# is 180 degrees out of phase with C. C and C# may be tied HIGH to force the use of K and K# as the output reference clocks instead of having to provide C and C# clocks. If tied HIGH, these inputs may not be allowed to toggle during device operation.
10R 11R	TMS TDI	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 2.5V I/O levels. These pins may be left Not Connected if the JTAG function is not used in the circuit.
2R	TCK	Input	IEEE 1149.1 Clock Input: JEDEC-standard 2.5V I/O levels. This pin must be tied to V_{SS} if the JTAG function is not used in the circuit.
2H, 10H	V_{REF}	Input	HSTL Input Reference Voltage: Nominally $V_{DD}Q/2$ but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffer trip point.
11H	ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 x RQ, where RQ is a resistor from this pin to ground. Alternately, this pin can be connected directly to V_{DD}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

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PIN DESCRIPTIONS (continued)

PINS (x18)	SYMBOL	TYPE	DESCRIPTION
10P 11N 11M 10K 11J 11G 10E 11D 11C 3B 3C 2D 3F 2G 3J 3L 3M 2N	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17	Input	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations.
1A, 11A	DNU	Output	Do Not Use. These pins should not be used.
1R	TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.
11P 10M 11L 11K 10J 11F 11E 10C 11B 2B 3D 3E 2F 3G 3K 2L 3N 3P	Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17	Output	Synchronous Data Outputs: Output data is synchronized to the respective C and C# or to K and K# rising edges if C and C# are tied HIGH. This bus operates in response to R# commands.
5F, 7F, 5G, 7G, 5H, 7H, 5J,7J, 5K, 7K	V_{DD}	Supply	Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range.
4E, 8E, 4F, 8F, 4G, 8G, 3H, 4H, 8H, 9H, 4J, 8J, 4K, 8K, 4L, 8L	$V_{DD}Q$	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. See DC Electrical Characteristics and Operating Conditions for range.

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PIN DESCRIPTIONS (continued)

PINS (x18)	SYMBOL	TYPE	DESCRIPTION
2A, 10A, 4C, 8C, 4D-8D, 5E-7E, 6F, 6G, 6H, 6J, 6K, 5L-7L, 4M-8M, 4N, 8N	V_{SS}	Supply	Power Supply: GND.
3A, 7A, 9A, 1B, 5B, 9B, 10B, 1C, 2C, 9C, 1D, 9D, 10D, 1E, 2E, 9E, 1F, 9F, 10F, 1G, 9G, 10G, 1H, 1J, 2J, 9J, 1K, 2K, 9K, 1L, 2K, 10L, 1M, 2M, 9M, 1N, 9N, 10N, 1P, 2P, 9P	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

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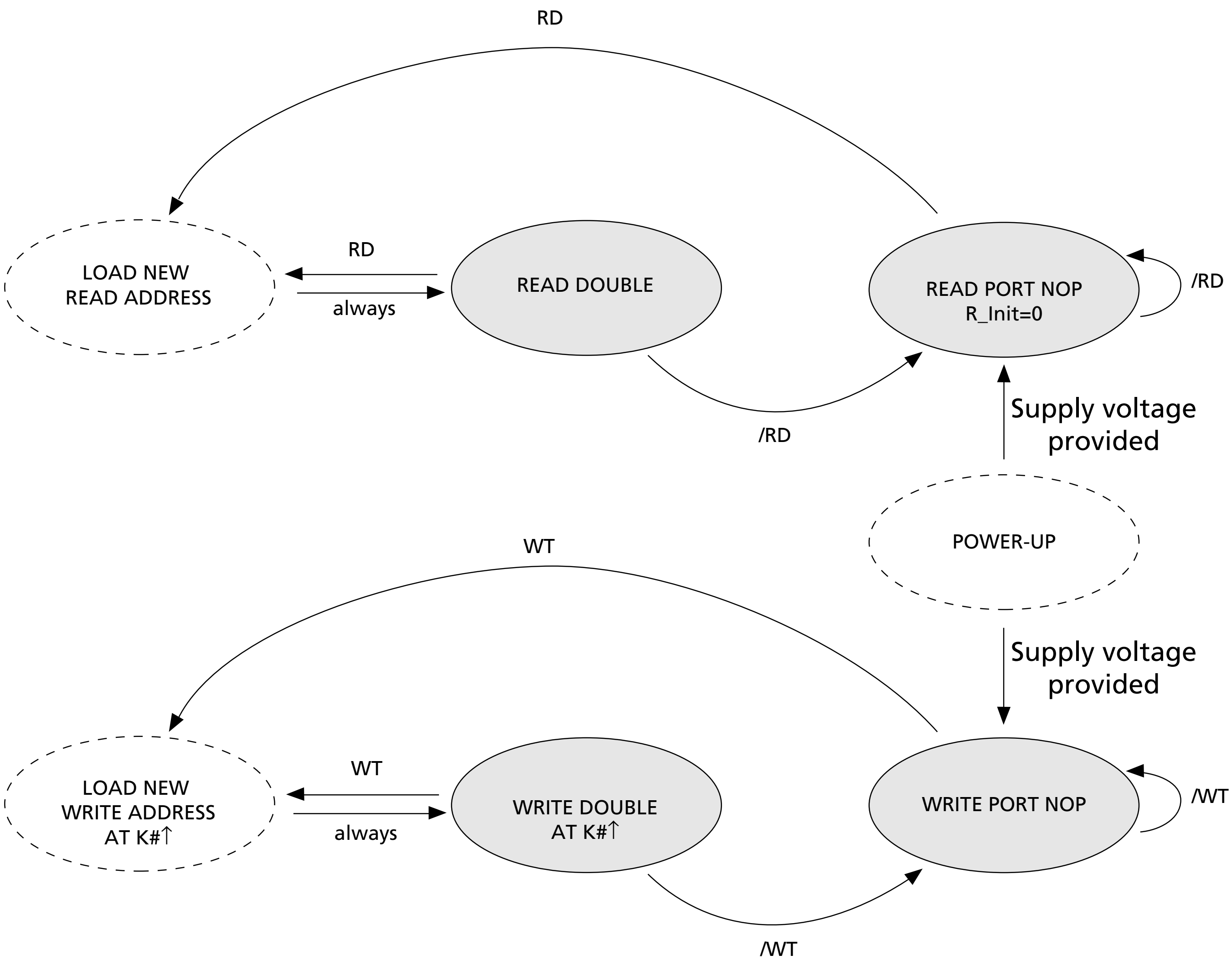
BUS CYCLE STATE DIAGRAM



NOTE:
1. The address is concatenated with 1 additional internal LSB to facilitate burst operation. The address order is always fixed as: xxx...xxx+0, xxx...xxx+1. Bus cycle is terminated at the end of this sequence (burst count = 2).
2. State transitions: RD = (R# = LOW); WT = (W# = LOW).
3. Read and write state machines can be active simultaneously.
4. State machine control timing sequence is controlled by K.

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TRUTH TABLE

(Notes 1-6)

OPERATION	K	R#	W#	D OR Q	D OR Q
WRITE Cycle: Load address, input write data on consecutive K and K# rising edges	L→H	X	L	DA(A+0) at K(t)↑	DA(A+1) at K#(t)↑
READ Cycle: Load address, output data on consecutive C AND C# rising edges	L→H	L	X	QA(A+0) at C(t+1)↑	QA(A+1) at C#(t+1)↑
NOP: No operation	L→H	H	H	D = X Q = High-Z	D = X Q = High-Z
STANDBY: Clock stopped	Stopped	X	X	Previous State	Previous State

BYTE WRITE OPERATION[7]

OPERATION	K	K#	BW0#	BW1#
WRITE D0-17 at K rising edge	L→H		0	0
WRITE D0-17 at K# rising edge		L→H	0	0
WRITE D0-8 at K rising edge	L→H		0	1
WRITE D0-8 at K# rising edge		L→H	0	1
WRITE D9-17 at K rising edge	L→H		1	0
WRITE D9-17 at K# rising edge		L→H	1	0
WRITE nothing at K rising edge	L→H		1	1
WRITE nothing at K# rising edge		L→H	1	1

NOTE:
1. X means “Don’t Care.” H means logic HIGH. L means logic LOW. ↑ means rising edge; ↓ means falling edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges except if C and C# are HIGH then data outputs are delivered at K and K# rising edges.
3. R# and W# must meet setup/hold times around the rising edge (LOW to HIGH) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. It is recommended that K = /K# = C = /C# when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.
7. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} .... -0.5V to +3.6V
Voltage on $V_{DD}Q$ Supply
Relative to V_{SS} .... -0.5V to V_{DD}
V_{IN} .... -0.5V to V_{DD} + 0.5V
Storage Temperature .... -55°C to +125°C
Junction Temperature** .... +125°C
Short Circuit Output Current .... ±70mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C; +2.4V ≤ V_{DD} ≤ +2.6V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	V_{REF} + 0.1	$V_{DD}Q$ + 0.3	V	3, 4
Input Low (Logic 0) Voltage		V_{IL}	-0.3	V_{REF} - 0.1	V	3, 4
Clock Input Signal Voltage		V_{IN}	-0.3	$V_{DD}Q$ + 0.3	V	3, 4
Input Leakage Current	0V ≤ V_{IN} ≤ $V_{DD}Q$	IL_I	-5	5	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (Q)	IL_O	-5	5	µA	
Output High Voltage	$\|I_{OH}\|$ ≤ 0.1mA	V_{OH} (LOW)	$V_{DD}Q$ - 0.2	$V_{DD}Q$	V	3, 5, 7
	Note 1	V_{OH}	$V_{DD}Q$/2 - 0.08	$V_{DD}Q$/2 + 0.08	V	3, 5, 7
Output Low Voltage	I_{OL} ≤ 0.1mA	V_{OL} (LOW)	V_{SS}	0.2	V	3, 5, 7
	Note 2	V_{OL}	$V_{DD}Q$/2 - 0.08	$V_{DD}Q$/2 + 0.08	V	3, 5, 7
Supply Voltage		V_{DD}	2.4	2.6	V	3
Isolated Output Buffer Supply		$V_{DD}Q$	1.4	1.6	V	3, 6
Reference Voltage		V_{REF}	0.68	0.9	V	3

NOTE:
1. Outputs are impedance-controlled. | I_{OH} | = ($V_{DD}Q$/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
2. Outputs are impedance-controlled. I_{OL} = ($V_{DD}Q$/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
3. All voltages referenced to V_{SS} (GND).
4. Overshoot: V_{IH} (AC) ≤ V_{DD} + 0.7V for t ≤ ^tKHKH/2
   Undershoot: V_{IL} (AC) ≥ -0.5V for t ≤ ^tKHKH/2
   Power-up: V_{IH} ≤ $V_{DD}Q$ + 0.3V and V_{DD} ≤ 2.4V and $V_{DD}Q$ ≤ 1.4V for t ≤ 200ms
   During normal operation, $V_{DD}Q$ must not exceed V_{DD}. R# and W# signals may not have pulse widths less than ^tKHKL (MIN) or operate at cycle rates less than ^tKHKH (MIN).
5. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. For higher $V_{DD}Q$ voltages, contact factory for product information.
7. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

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I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(+20°C ≤ T_J ≤ +110°C; V_{DD} = MAX unless otherwise noted)

				MAX				
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-6	-7.5	-10	UNITS	NOTES
Operating Supply Current: DDR	All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKHKH (MIN); Outputs open	I_{DD}	TBD	500	400	300	mA	1, 2, 3
Standby Supply Current: NOP	^tKHKH = ^tKHKH (MIN); Device in NOP state; All addresses/data static	I_{SB1}	TBD	170	140	110	mA	2, 4
Output Supply Current: DDR (For information only)	C_L = 15pF	$I_{DD}Q$		34	27	20	mA	5

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	4	5	pF	6
Input, Output Capacitance (D, Q)		C_O	6	7	pF	6
Clock Capacitance		C_{CK}	5	6	pF	6

THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ_{JA}	25	°C/W	6, 7
Junction to Case (Top)		θ_{JC}	10	°C/W	6
Junction to Pins (Bottom)		θ_{JB}	12	°C/W	6, 8

NOTE:
1. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading. Typical value is measured at 6ns cycle time.
2. Typical values are measured at V_{DD} = 2.5V, $V_{DD}Q$ = 1.5V and temperature = 25°C.
3. Operating supply currents and burst mode currents are calculated with 50 percent READ cycles and 50 percent WRITE cycles.
4. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
5. Average I/O current and power is provided for information purposes only and is not tested. Calculation assumes that all outputs are loaded with C_L (in farads), f = input clock frequency, half of outputs toggle at each transition (n=18), $V_{DD}Q$=1.5V and uses the equations: Average I/O Power as dissipated by the SRAM is: $P = 0.5 * n * f * C_L * V_{DD}Q^2$. Average $I_{DD}Q = n * f * C_L * V_{DD}Q$.
6. This parameter is sampled.
7. Average thermal resistance between the die and the case top surface per MIL SPEC 883 Method 1012.1.
8. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.

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AC ELECTRICAL CHARACTERISTICS

(Notes 1, 4, 5, 7); (+20°C ≤ T_J ≤ +110°C; +2.4V ≤ V_{DD} ≤ +2.6V)

DESCRIPTION	SYMBOL	-6		-7.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock cycle time (K, K#, C, C#)	^{t}KHKH	6.0		7.5		10		ns	
Clock HIGH time (K, K#, C, C#)	^{t}KHKL	2.4		3.0		3.5		ns	
Clock LOW time (K, K#, C, C#)	^{t}KLKH	2.4		3.0		3.5		ns	
Clock to clock# (K↑→K#↑, C↑→C#↑)	^{t}KHK#H	2.7	3.3	3.4	4.1	4.6	5.4	ns	
Clock to data clock (K↑→C↑, K#↑→C#↑)	^{t}KHCH	0.0	2.0	0.0	2.5	0.0	3.0	ns	
Output Times									
C, C# HIGH to output valid	^{t}CHQV		2.5		3.0		3.0	ns	
C, C# HIGH to output hold	^{t}CHQX	1.2		1.2		1.2		ns	
C HIGH to output High-Z	^{t}CHQZ		2.5		3.0		3.0	ns	2,6
C HIGH to output Low-Z	^{t}CHQX1	1.2		1.2		1.2		ns	2,6
Setup Times									
Address valid to K rising edge	^{t}AVKH	0.7		0.8		1.0		ns	3
Control inputs valid to K rising edge	^{t}IVKH	0.7		0.8		1.0		ns	3
Data-in valid to K, K# rising edge	^{t}DVKH	0.7		0.8		1.0		ns	3
Hold Times									
K rising edge to address hold	^{t}KHAX	0.7		0.8		1.0		ns	3
K rising edge to control inputs hold	^{t}KHIX	0.7		0.8		1.0		ns	3
K, K# rising edge to data-in hold	^{t}KHDX	0.7		0.8		1.0		ns	3

NOTE:
1. This parameter is sampled.
2. Transition is measured ±100mV from steady state voltage.
3. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.
4. Test conditions as specified with the output loading as shown in Figure 1 unless otherwise noted.
5. Control input signals may not be operated with pulse widths less than ^{t}KHKL (MIN).
6. ^{t}CHQX1 is greater than ^{t}CHQZ at any given voltage and temperature.
7. If C, C# are tied HIGH, K, K# become the references for C, C# timing parameters.

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AC TEST CONDITIONS

Input pulse levels	0.25V to 1.25V
Input rise and fall times	0.3ns
Input timing reference levels	0.75V
Output reference levels	VDDQ/2
ZQ for 50Ω impedance	250Ω
Output load	See Figure 1

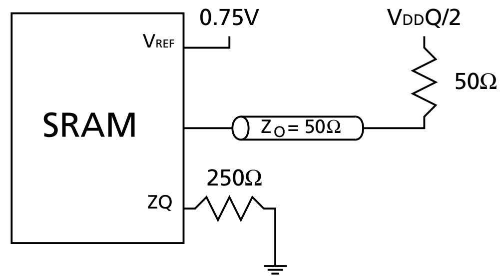

Figure 1
Output Load Equivalent

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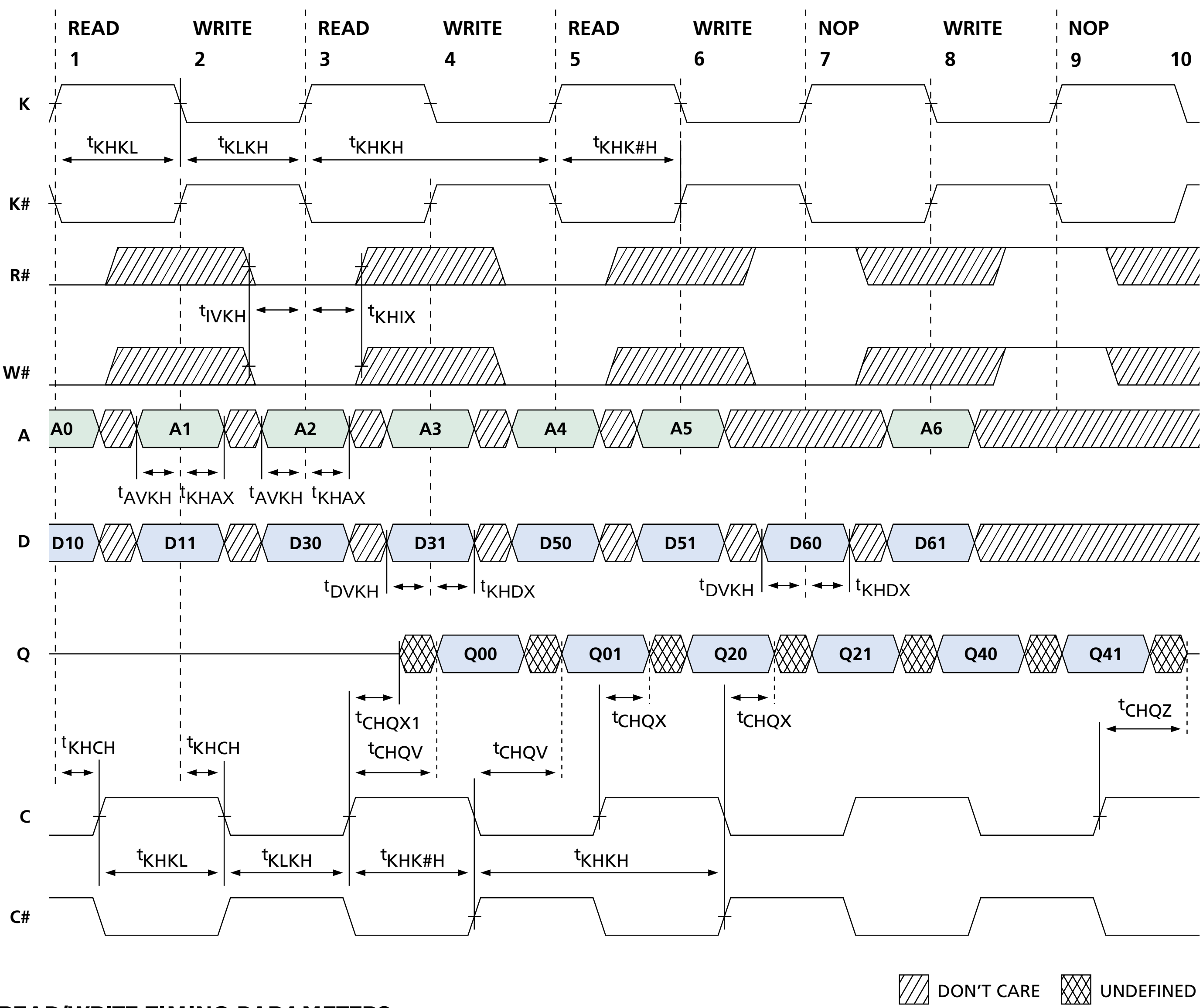
READ/WRITE TIMING



READ/WRITE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tKHKH	6.0		7.5		10		ns
tKHKL	2.4		3.0		3.5		ns
tKLKH	2.4		3.0		3.5		ns
tKHK#H	2.7	3.3	3.4	4.1	4.6	5.4	ns
tKHCH	0.0	2.0	0.0	2.5	0.0	3.0	ns
tCHQV		2.5		3.0		3.0	ns
tCHQX	1.2		1.2		1.2		ns
tCHQZ		2.5		3.0		3.0	ns

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tCHQX1	1.2		1.2		1.2		ns
tAVKH	0.7		0.8		1.0		ns
tIVKH	0.7		0.8		1.0		ns
tDVKH	0.7		0.8		1.0		ns
tKHAX	0.7		0.8		1.0		ns
tKHIX	0.7		0.8		1.0		ns
tKHDX	0.7		0.8		1.0		ns

NOTE:
1. Q00 refers to output from address A0+0. Q01 refers to output from the next internal burst address following A0, i.e., A0+1.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. In this example, if address A0 = A1, data Q00 = D10, Q01 = D11. Write data is forwarded immediately as read results.

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IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The QDR SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

DISABLING THE JTAG FEATURE

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 2. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 3.)

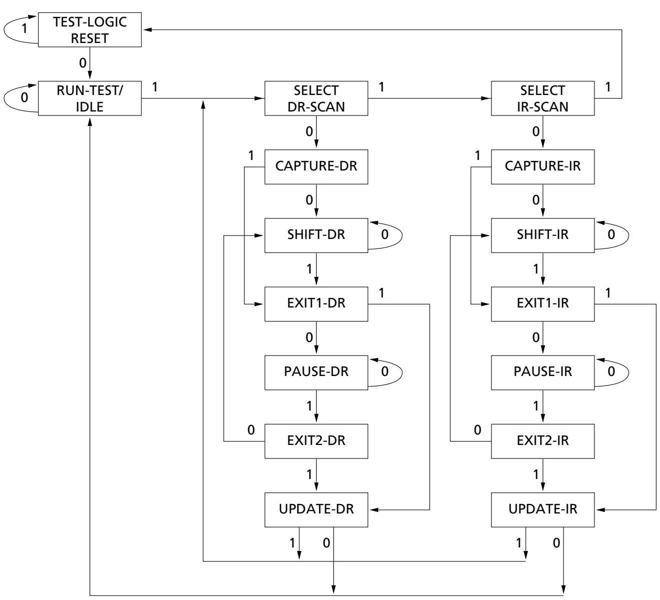

Figure 2
TAP Controller State Diagram

NOTE: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

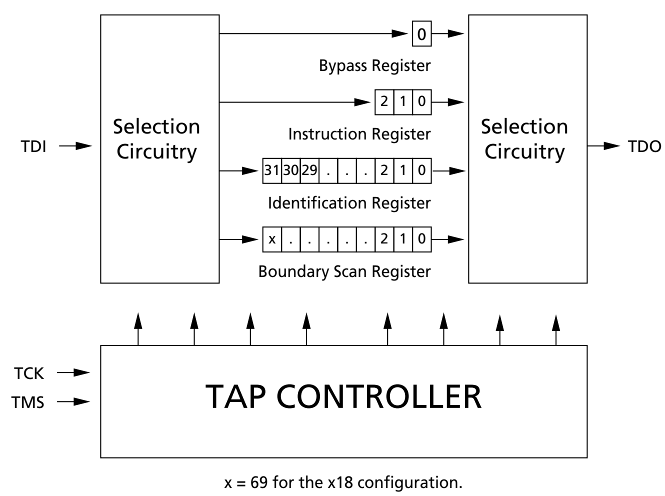

Figure 3
TAP Controller Block Diagram

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TEST DATA-OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 2.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 3.)

PERFORMING A TAP RESET

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

INSTRUCTION REGISTER

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 2. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins. The x18 configuration has a 69-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table shows the order in which the bits are connected. Each bit corresponds to one of the pins on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET

OVERVIEW

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

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EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, hence this device is not IEEE 1149.1 compliant.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. EXTEST does not place the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bi-directional pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instruction are not implemented but are reserved for future use. Do not use these instructions.

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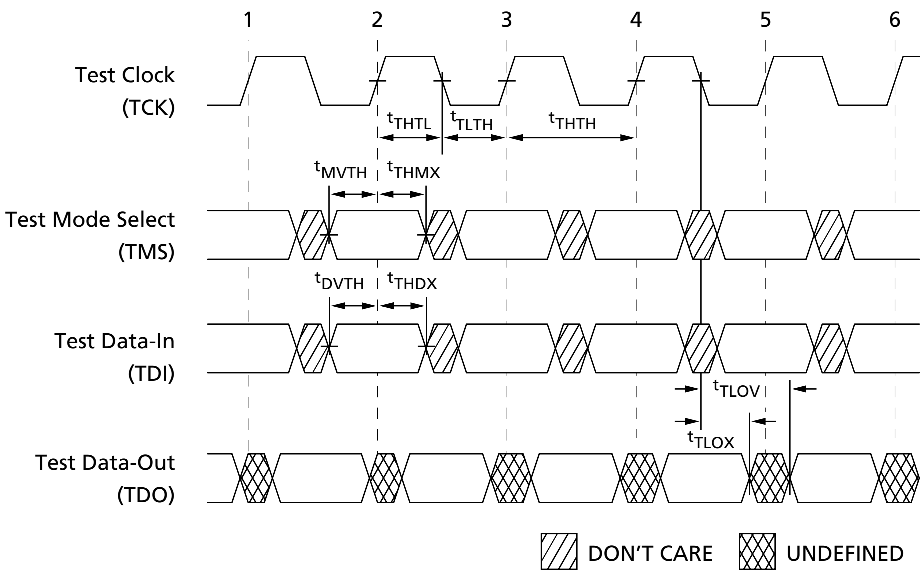
TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) (+20°C ≤ T_J ≤ +100°C, +2.4V ≤ V_{DD} ≤ +2.6V)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 4.

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TAP AC TEST CONDITIONS

Input pulse levels	V_{SS} to 2.5V
Input rise and fall times	1ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Test load termination supply voltage	1.25V

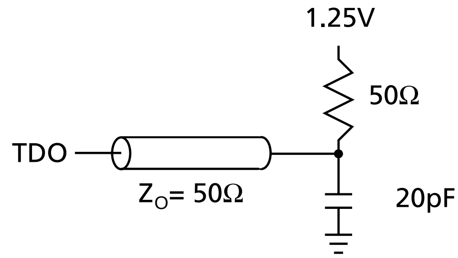

Figure 4
Tap AC Output Load Equivalent

TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C, +2.4V ≤ V_{DD} ≤ +2.6V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$	I_{LO}	-5.0	5.0	µA	
Output Low Voltage	I_{OLC} = 100µA	V_{OL1}		0.2	V	1
Output Low Voltage	I_{OLT} = 2mA	V_{OL2}		0.7	V	1
Output High Voltage	$\|I_{OHC}\|$ = 100µA	V_{OH1}	2.1		V	1
Output High Voltage	$\|I_{OHT}\|$ = 2mA	V_{OH2}	1.7		V	1

NOTE: 1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} (AC) ≤ V_{DD} + 0.7V for t ≤ $^tKHKH/2$
Undershoot: V_{IL} (AC) ≥ -0.5V for t ≤ $^tKHKH/2$
Power-up: V_{IH} ≤ +2.6V and V_{DD} ≤ 2.4V and $V_{DD}Q$ ≤ 1.4V for t ≤ 200ms
During normal operation, $V_{DD}Q$ must not exceed V_{DD}. Control input signals (such as LD#, R/W#, etc.) may not have pulse widths less than ^tKHKL (MIN) or operate at frequencies exceeding ^fKF (MAX).

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IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	512K x 18	DESCRIPTION
REVISION NUMBER (31:29)	000	Version number.
DEVICE ID (28:12)	00011000010000000	512K x 18 QDR 2-word burst.
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE (x18)
Instruction	3
Bypass	1
ID	32
Boundary Scan	69

INSTRUCTION CODES

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect SRAM operations. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

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Boundary Scan (Exit) Order

BIT#	SIGNAL NAME	PIN ID
1	C#	6R
2	C	6P
3	SA	6N
4	SA	7P
5	SA	7N
6	SA	7R
7	SA	8R
8	SA	8P
9	SA	9R
10	D0	10P
11	Q0	11P
12	D1	11N
13	Q1	10M
14	D2	11M
15	Q2	11L
16	D3	10K
17	Q3	11K
18	D4	11J
19	ZQ	11H
20	Q4	10J
21	D5	11G
22	Q5	11F
23	D6	10E
24	Q6	11E
25	D7	11D
26	Q7	10C
27	D8	11C
28	Q8	11B
29	Reserved	11A; reads as X
30	GND/SA20	10A; reads as 0
31	NC/SA18	9A; reads as 1
32	SA	8B
33	SA	7C
34	SA	6C
35	R#	8A

BIT#	SIGNAL NAME	PIN ID
36	BW0#	7B
37	K	6B
38	K#	6A
39	BW1#	5A
40	W#	4A
41	SA	5C
42	SA	4B
43	NC/SA19	3A; reads as 1
44	GND/SA21	2A; reads as 0
45	Reserved	1A; reads as X
46	D9	3B
47	Q9	2B
48	D10	3C
49	Q10	3D
50	D11	2D
51	Q11	3E
52	D12	3F
53	Q12	2F
54	D13	2G
55	Q13	3G
56	D14	3J
57	Q14	3K
58	D15	3L
59	Q15	2L
60	D16	3M
61	Q16	3N
62	D17	2N
63	Q17	3P
64	SA	3R
65	SA	4R
66	SA	4P
67	SA	5P
68	SA	5N
69	SA	5R

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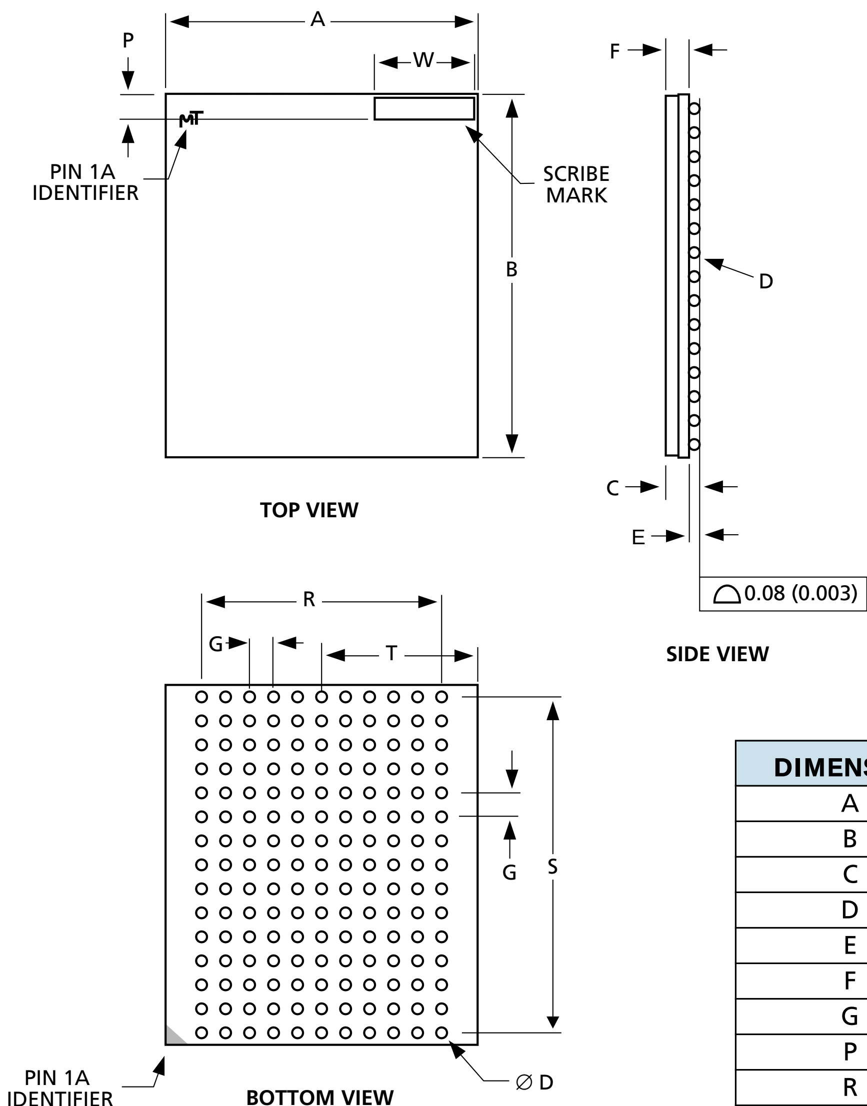
165-PIN FBGA



NOTE: 1. Controlling dimensions are metric.
2. Molding dimensions do not include protrusion; allowable mold protrusion is 0.25mm per side.

DIMENSIONS

DIMENSION	mm	INCHES	NOTE
A	13.0±0.1		
B	15.0±0.1		
C	1.20		Max
D	0.45±0.05		
E	0.45		Max
F	0.850±0.075		
G	1.00		Typical
P	1.00		Typical
R	10.00		Typical
S	14.00		Typical
T	6.50		Typical
W	4.40		Max

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