Memory Technologies Study Guide

1) Acronyms
   a) ROM - Read Only Memory (mask programmed ROM - contents determined at manufacture time, never changed).
   b) RAM - Random Access Memory
   c) DRAM - Dynamic RAM (1 transistor + 1 capacitor per memory cell), memory cell needs to periodically refreshed
   d) SRAM - Static RAM (6 transistors per memory cell)
   e) SDRAM- Synchronous DRAM (DRAM with clock)
   f) SSRAM - Synchronous SRAM (SRAM with clock)
   g) DDR- SDRAM - Double Data Rate SDRAM (data transferred on both clock edges)
   h) PROM - Programmable ROM (ROM programmed on user desktop), usually One Time Programmable (OTP)
   i) EEPROM - Electrically Erasable PROM
   j) Flash RAM - Non-volatile RAM, blocks of RAM can be erased, can also be programmed via single locations
   k) RDRAM - Rambus DRAM -- DRAM with very different interface from normal DRAM.
   l) Dual Port SRAM - SRAM with two ports (two sets of address lines, two sets of data buses). Reads/Writes to different memory locations can occur simultaneously.

2) Non-Volatile Memories -- ROM, PROM, EEPROM, Flash RAM
3) Volatile Memories - all SRAM, DRAM types
4) Main Memory (non-cache) technologies : all DRAM types (high density, but slow)
5) Cache Memory technologies : All SRAM types
6) Synchronous vs Non-synchronous memories : the addition of a clock allows faster operation generally for burst mode operation. The clock signal also allows easy integration of a counter inside the memory device to provide address generation for burst mode addresses (uP provides first address, memory device generates subsequent addresses). Finally a clock signal means that all control lines, address lines, data lines only have to satisfy setup/hold times around the active clock edge and that these signals are latched on the active clock edge inside the device. DDR- DRAMs latch data/control signals on both edges of the clock.
7) RDRAM - Rambus DRAM -- uses limited swing signaling technology to achieve a high bus rate (400 Mhz clock). Data transfer on both edges of clock over a 2 Byte-wide data bus to achieve 1.6 Gbyte/sec transfer rate. The devices have no chip selects - each device has an 'ID' and a data access operation involves transmission of the Device ID + address + R/W operation select over the control bus (8-bit bus). The device whose ID matches the ID in the control packet responds to the operations. RDRAM has bus bandwidth at the cost of high latency. The only effective transfers to RDRAM are block transfers.
8) Cache vs Main Memory --- All transfers between cache and Main Memory involve block transfers (multiple bytes) so main memory technologies optimize block transfers instead of random accesses to individual words. Accesses to cache are both block transfers and random accesses to words, so cache memory technologies need to have fast random access. DRAM technologies used for main memory, SRAM technologies for caches.
9) DRAMs multiplex the address between row/column addresses; they only have half the number of address pins that you might expect for the device. The RAS# (Row Address Strobe) and CAS# (Column addresss strobe) are the control signals used to latch in the Row, Column addresses.