EE 3724 Test #1 Solutions - Summer '00 – Reese

1. (9 pts) The three parts of any computer is Memory, Control, and Input/Output. Explain the function of each.

   a) Memory - *where instructions and data are stored for the computer*

   b) Input/Output - *computer's means of interacting with the external world*

   c) Control - *logic that controls fetching and execution of instructions*

2) 5 pts. What is an instruction mnemonic? Give an example.
   A mnemonic is the human-readable notation for an instruction, such as MOV AX, BX

3) 5 pts. What is the function of an instruction pointer register in a processor?
   It is a register that contains the address of the next instruction to be executed.

4) 6 pts. A memory device has two busses that are used to communicate with it -- explain what these busses are and give an example of a memory device.
   Address bus – specifies the location that is to be read/written
   Data bus – specifies the data being written
   A 16x8 memory device contains 16 locations (4 address lines), with 8 data bits per location (data bus is 8 bits wide).

5) 5 pts. What does 'assembly' mean?
   Assembly is the conversion of an instruction mnemonic to its machine code representation (binary representation).

6) 5 pts. What does 'disassembly' mean?
   Disassembly is the conversion from machine code to instruction mnemonics.

7) 10 pts. Assume I am building a custom processor to solve a problem. My processor will have 9 different instructions, will have one four bit register inside of it besides the program counter, and any programs written for the processor will be at most 50 instructions long. Assume the format for the machine code for each instruction will be :

   OPCODE | DATA

   Where the opcode specifies the instruction, and the data specifies either an address or data for one of the registers.

   How many bits would you use to encode the machine code for the instructions of this processor? JUSTIFY YOUR ANSWER or YOU WILL GET ZERO CREDIT!!!!!!!!!!!!!!

   The opcode field must be at least 4 bits wide to encode 9 instructions ($2^4 = 16$).
   The data field must contain both data and address information. The data register is 4 bits wide; address for programs up to 50 instructions must be at least 6 bits wide ($2^6 = 64$). So data field is maximum (4,6) = 6 bits wide.

   Total instruction width is 4 bits (opcode) + 6 bits (data) = 10 bits.

8) 5 pts Convert the decimal value -48 to a 16-bit 2'complement hex number.
*Magnitude of 48 in 8-bits is 30h (3*16+0). Decimal value was negative, so Take 2's complement = D9h. Sign extend to 16 bits = FFD0h.*

9) 5 pts. The following number 81h represents a decimal number in 8 bit, 2's complement format. What is its decimal value?
Will be a negative number since MSB=1. Take 2's complement of 81h to get magnitude = 7Fh = 127. Final answer is –127 decimal.

10) 5 pts. What is the ASCII code used for*? It is a 7-bit code for character data, English alphabet.*

11) 12 pts.
Assume the following memory contents:

Address Contents

09A0:0000	C5	67	A5	00	12	BC	34	BB	F4	72	09	A3	29	01	D4	CE
09A0:0010	FE	89	02	D8	A4	8A	7C	DD	90	3C	9B	83	65	19	F6	8A
09A0:0020	A7	CC	9A	BD	8E	90	2C	00	1C	90	0E	13	8C	39	58	C6
09A0:0030	76	D7	CA	FF	D8	71	18	24	40	A8	2C	76	93	C5	0F	9E
09A0:0040	82	A6	54	2E	9A	20	0A	98	E4	A0	0E	25	38	29	2C	86

. Assume the following register contents:
DS: 09A2, SS: 09A0, ES: 09A1, BX= 000F, BP:0012, SI: 0008, DI:0004, CX: 0002

Give the final value of the affected register:

a) mov al, [SI] *[DS:SI] =[09A2:0008] = [09A0:0028] , AL=1C*

b) mov cx, [BX+3] *[DS:BX+3] = [09A2:000F+3] =[09A2:0012] = [09A0:0032], AX= FFCA*

c) mov dl, [BP+8] *[SS:BP+8] =[09A0:0012+8]=[09A0:001A], dl = 9B*

12) 5 pts. For the register contents in the previous example, what is the 20-bit PHYSICAL address for DS:BX ??? *09A20+ 0000F = 09A2F*

13) 8 pts. Assume the following register contents:

Assume the following register contents:
DS: 09A2, SS: 09A0, ES: 09A1, BX= 000F, BP:0012, SI: 0008, DI:0004, CX: 0002
EAX = AA2387E4

Address	Contents															
09A0:0000																
09A0:0010					*E4*	*87*										
09A0:0020													*E4*			
09A0:0030																
09A0:0040																

Show how memory is modified for the following instructions:

a) mov [bp+2], ax *[SS:BP+2]=[09A0:0012+2] = [09A0:0014] , Write bytes E4, 87*

b) mov [bx-2], al *[DS:BX-2]=[09A2:000F-2]=[09A2:000D]=[09A0:002D], write E4.*

14) 10 pts. Assume the following register, memory contents.

Address	Contents															
09A0:0000	C5	67	A5	00	12	BC	34	BB	F4	72	09	A3	29	01	D4	CE
09A0:0010	FE	89	02	D8	A4	8A	7C	DD	90	3C	9B	83	65	19	F6	8A
09A0:0020	A7	CC	9A	BD	8E	90	2C	00	1C	90	0E	13	8C	39	58	C6
09A0:0030	76	D7	CA	FF	D8	71	18	24	40	A8	2C	76	93	C5	0F	9E
09A0:0040	82	A6	54	2E	9A	20	0A	98	E4	A0	0E	25	38	29	2C	86

. Assume the following register contents:
DS: 09A2, SS: 09A0, ES: 09A1, BX= 000F, BP:0012, SI: 0008, DI:0004, CX: 0002

For the following two instruction program, show how memory is modified, AND give the FINAL values of any registers that change after execution of these two instructions:

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Cld
Rep  movsb
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CX=2, read two bytes starting from [DS:SI] and write to [ES:DI]
1s byte: [DS:SI] = [09A2:0008] = [09A0:0028] = 1C, 2nd byte is [09A2:0009] = 90
Written to
1st byte to [ES:DI] = [09A1:0004]=[09A0:0014], 2nd byte to [09A1:005].
New memory contents:

09A0:0010	FE	89	02	D8	*1C*	*90*	7C	DD	90	3C	9B	83	65	19	F6	8A

Final value of SI = 000A, DI=0006, CX=0000.

15) 5 pts. Give any four 1-bit flags that are contained in the FLAG register of the x86 and explain their meanings.
Carry flag = set when carry out of MSB of operation
Zero flag = set when operation result is zero
Overflow Flag = set when operation produces a 2's complement overflow
Negative flag = set when operation produces a value whose MSB = 1
Direction Flag = controls whether SI/DI are incremented/decremented during string instructions.