EE 3724 Test #3 Solutions- Spring '01 – Reese

1. (4 pts) Why it is important that main memory support efficient block transfers?
   There is cache between main memory and the processor. The cache gets information from main memory, and always transfers a block of data from main memory, because if a word in the block is currently needed, then there is a high probability that a nearby word is also needed.

2. (4 pts) Why is DRAM denser than SRAM? Be explicit.
   SRAM requires 6 transistors per memory cell, DRAM requires 1 transistor and 1 small capacitor. DRAM memory cells take less silicon area, so more memory cells can be packed into the same area.

3. (4 pts) What memory type multiplexes the address between row and column addresses?
   DRAM, SDRAM

4. (4 pts) For problem (3), why is the address bus multiplexed between row and column addresses?
   This reduces the number of needed address pins by a factor of 2, so the DRAM package is smaller which allows more to DRAM chips to fit in a given space (on a SIMM or DIMM).

5. (4 pts) Would a burst mode transfer be supported in an SSRAM or an SRAM?
   An SSRAM supports burst mode (S = Synchronous = clock pin), an SRAM would not.

6. (4 pts) What is special about the electrical signaling used on RDRAM that is different from all of the other memory types studied (Hint: it is one of the reasons for the high bandwidth of the RDRAM).
   RDRAM uses limited swing voltage signaling -- the signals swing +/- 200 mv about a fixed reference voltage. Less voltage swing means higher speed signaling.

7. (4 pts) Given an interrupt number of 0x10h, what would the address of Interrupt Service Routine be in the Interrupt vector table?
   *Address of ISR in the vector table = 0x10 * 4 = 0x0040*

8. (4 pts) Why is a special IRET instruction needed for an interrupt service routine. Why can't we just just a normal 'RET' instruction?
   The IRET is needed because it pops off the FLAGS register from the stack in addition to the CS, IP. Recall that the flags register, CS, IP are automatically pushed on the stack during an interrupt service.

9. (4 pts) What does the term 'refresh' mean with respect to DRAM?
   Since a capacitor is the basis of DRAM cells they leak over time. Refresh means that the DRAM controller accesses each ROW of DRAM cells every so often in order to recharge the capacitor values of the row cells.

10. (4 pts) What is an interrupt acknowledge cycle used for after an INTR interrupt has been recognized?
   This cycle fetches the interrupt number from the lower 8 data lines. The interrupt number is provided by the interrupting device. This number is then used to calculate the address of the ISR in the interrupt vector table.

11. (6 pts) For the 8255A, assume the following port locations: Port A: 0520h, Port B: 0524h, Port C: 0528h, Control: 052Ch. Write an instruction sequence that will configure Port A as an OUTPUT, Port B as an INPUT, Lower half of Port C as an OUTPUT, and Upper Half of port C as an INTPUT. Use MODE 0 for all ports.

mov dx, 052ch
mov al, 10001010b
out dx, al

12. (6 pts) For 8255A, and assuming the port definitions above, write an instruction sequence that will read a byte from Port B and then write that byte to Port B (*mistake - should have been write byte to Port A*)

mov dx, 0524h
in al, dx
mov dx, 0520h
out dx, al

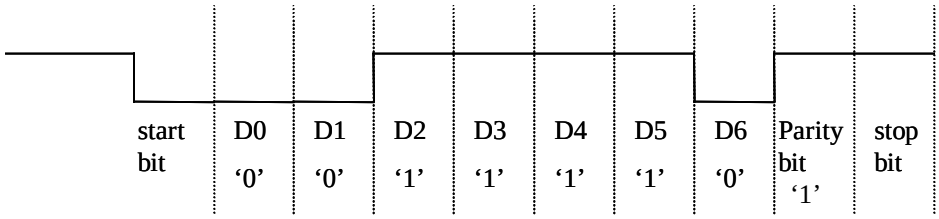
13. (6 pts) For the 8255A, and assuming the port definitions above, write an instruction sequence that will output C7 (MSB of port C) to a '1', then to a '0', WITHOUT affecting any of the other port C output bits (hint: look at the function of the control register when the control register MSB is '0').

mov dx, 052Ch
mov al, 00001111h
out dx, al
mov al, 00001110h
out dx, al

14. (4 pts) Define the terms half-duplex and full-duplex?
half-duplex -- at any given time, data transfer is only in one direction (either receiving or transmitting, but not both at the same time).

f*ull-duplex - data transfer can occur in both directions at the same time.*

15. (4 pts) Draw the serial data waveform for sending the byte 3Ch assuming a data format of 7 data bits, Odd parity, 1 stop bit. Data is sent LSB first, use positive logic.
3Ch = 011 1100 parity bit = 1 since # of '1' bits is even we want odd parity.



16. (4 pts) Why is an INPUT FIFO included on the 16550D UART? Why is this a good idea?
An INPUT FIFO allows the processor extra time to fetch data from the UART, If the processor takes a little longer than normal in checking the UART for data, the FIFO provides some temporary storage space for capturing incoming data bytes, helping to prevent data overrun.

17. (12 pts) For the 16550D, assume the following port definitions:
Write a subroutine that will output the byte passed in 'AL' if the transmit register is empty (return with the carry flag = '0'). If the transmit register is not empty, return with the Carry flag = '1' and AL must have the original data that was passed to the subroutine.. Your subroutine should NOT wait until the transmit register is empty.

```
; all port definitions for COM1
rbr         equ   03f8h
thr         equ   03f8h
ier         equ   03f9h
iir         equ   03fAh
fcr         equ   03fAh
lcr         equ   03fBh
mcr         equ   03fCh
lsr         equ   03fDh
msr         equ   03feh
scr         equ   03ffh

dl_lsb      equ   03f8h
dl_msb      equ   03f9h
```

```
        mov  bl,   al           ; save byte to send
        mov  dx,  lsr           ; line status register
        in     al,   dx         ; read lsr
        test   al, 00100000h    ; check THRE bit = '1' if empty
        jz     full
        mov  al, bl             ; get byte back
        mov  dx, thr
        out    dx, al           ; output byte
        clc
        ret

full:
        mov al, bl
        stc
        ret
```

18. (4 pts) The RS232 standard only allows 10 bits to be transmitted in one serial "frame". What prevents us from transmitting 20 bits or 100 bits or 1000 bits in one frame?
RS232 is an asynchronous protocol which means the sending/receiving computers do not have a common clock. Slight differences in clock frequency on each side introduces error which sums over the time it takes to send a frame. Allowing only 10 bits means gives us a tolerance of approximately 5% in terms of clock difference between the sender/receiver. If we sent a longer frame, the clock error would build up over the frame to the point where we would not know where a 'bit' boundary was and we would get errors in transmission.

19. (9 pts) Define the terms "polled I/O" and "interrupt driven I/O". What is a problem with "polled I/O"?

Polled IO - processor continuously checks for data.
Interrupt driven IO -- processor is interrupted when data is ready.
Polled IO can be inefficient -- processor will either check too often or not often enough for data.

20. (4 pts)A "circular-buffer" is a data structure that we discussed in class. How can you tell if a circular buffer has data?
The circular buffer had data in it when the tail pointer was not equal to the head pointer.