Test 3 Study Guide

1. Be able to identify SSRAM, SRAM, DRAM, SDRAM, Dual Port SRAMs from pinout on datasheet. Be able to determine the memory organization (K x M) from pinout.
2. Know facts on memory data sheet.
3. Review hardware/software interrupts. Know reasons for steps in interrupt cycle. Know what an interrupt vector table is.
4. Know 2T and 4T bus cycles. Know what wait states are.
5. Be able to work problems similar to that found on homework #10.
6. Know what IN/OUT instructions do. Know parallel printer handshaking sequence.
7. Know the difference between polled and interrupt-driven IO.
8. Know what a circular buffer data structure is and what it is used for.
9. Know how to write an Interrupt Service Routine (ISR).
10. Know how hardware interrupts are generated via the INTR input to the 8086.
11. Know what fixed priority versus rotating priority means.
12. Know what the 8255 (Programmable Peripheral Interface) and 8259A (Programmable Interrupt Controller) were used for.

General: Expect to have a lot of short answer questions. You WILL be asked to write an ISR based on a circular buffer. You will NOT be able to use a calculator on the test. I will handout the same reference materials that I did last time.

WARNING: THIS IS NOT AN EXHAUSTIVE LIST OF TOPICS. You are responsible for everything we have covered since last test.