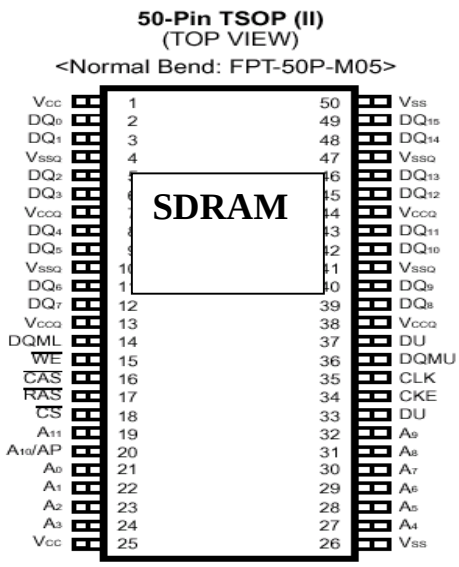
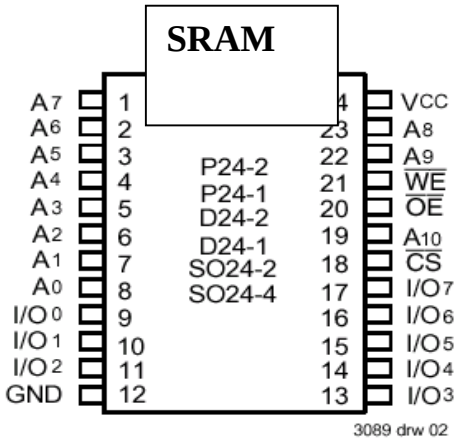
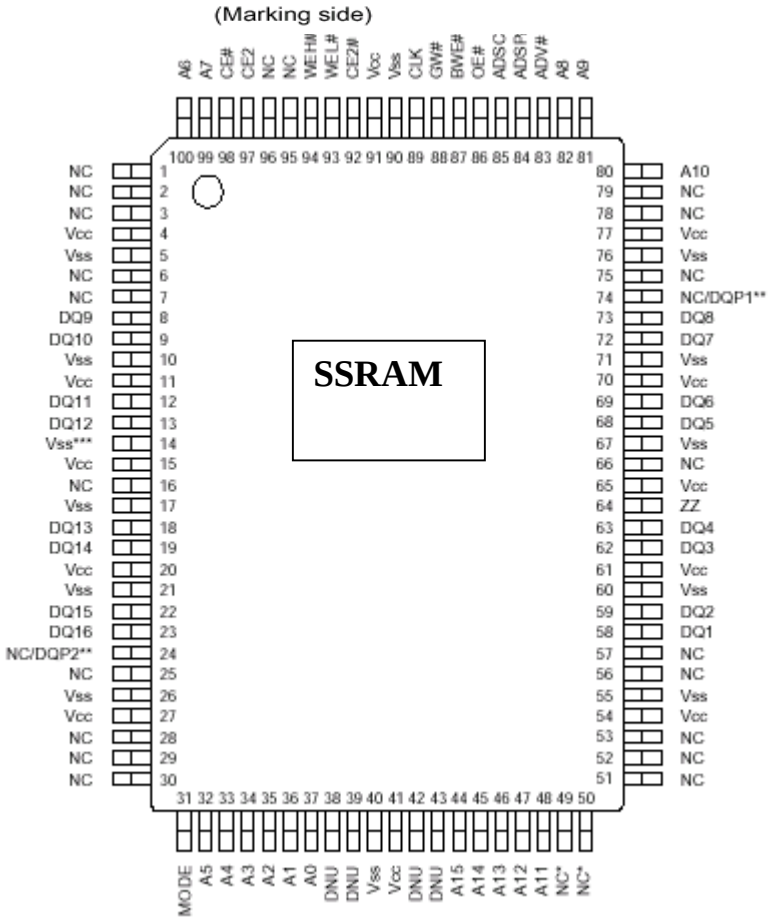
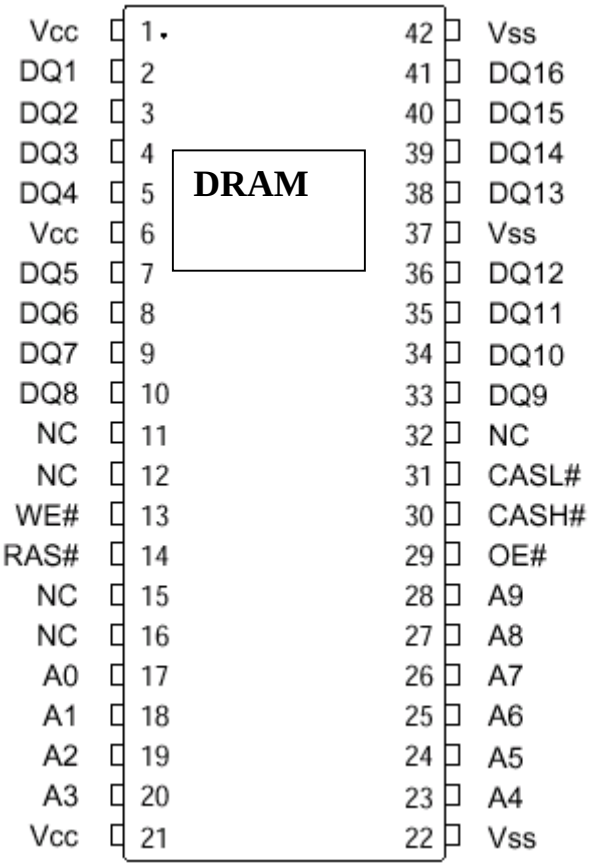
EE 3724 Test #3 - Summer '00 Solutions– Reese

1. (12 pts) Matchup each of the following pinouts below with one of the following: SDRAM, DRAM, SSRAM, SRAM.









2. (18 pts) For each of the following questions, use one or more of the following terms (they can be used more than once, put ALL applicable terms for an answer): SRAM, SSRAM, SDRAM, DRAM, RDRAM, Dual Port SRAM, EEPROM, Flash RAM

    a. Used for PC cache memory: SRAM, SSRAM
    b. Used as PC main memory: DRAM, SDRAM, RDRAM
    c. Non-volatile memory: EEPROM, Flash RAM
    d. New type of memory that uses device code sent on control bus instead of chip selects; has high bandwidth and high latency: RDRAM
    e. Basic memory cell has 6 transistors SRAM, SSRAM
    f. Basic memory cell is capacitor + 1 transistor DRAM, SDRAM, RDRAM
    g. Has a clock pin so that data is transferred synchronously instead of asynchronously SSRAM, SDRAM (also RDRAM)
    h. Two memory locations can be accessed simultaneously: dual port SRAM
    i. Memory contents need periodic refreshing: DRAM, SDRAM, RDRAM

3. (4 pts) An SRAM has address pins A0-A17, and Data pins D0-D15

    a. What is the organization (K x M) of this device? 256K x 16
    (18 address pins = $2^{18} = 2^8 * 2^{10} = 256 * 1K$)
    b. What is the total number of bits stored in this device? 4M
    (2^{18} x 16 = $2^{18} * 2^4 = 2^{22} = 2^2 * 2^{20} = 4 * 1$ M = 4M)

4. (6 pts) A burst transfer on a 486 processor (32-bit bus, 4 bytes) is characterized as 2-1-1-1 transfer.
    a. How many clocks does it take for this transfer? *5 clocks*
    b. How many bytes are transferred? *16 bytes (4 bytes in 2T, 4 bytes, 4 bytes, 4 bytes = 16 bytes)*
    c. How many clocks would it take to transfer the SAME number of bytes on the 486 if a 2T transfer was used for each word?
    16 bytes/ 4 bytes per 2t cycle = 4 2T cycles = 8 clocks.

5. (5 pts) Give the address decode equation for a 256Kbyte block of memory starting at location 40000h. Assume you have a maximum of 20 address lines (A0-A19).

   256K bytes = 218 = A0- A17. 40000 = 01xxxx….xxx = A19# A18

6. (8 pts) Give the value of the BE#3 to BE0# lines for each of the follow accesses (assume a 486 interface, uses a 32-bit wide data bus). Use 'H' or 'L' for the values.

	BE3#	BE2#	BE1#	BE0#
Mov ax,[302h]	L	L	H	H
Mov [224h],ax	H	H	L	L
In al, [587h]	L	H	H	H
Mov [370h],eax	L	L	L	L

7. (4 pts) Assume a 486 interface (32-bit bus). Give an instruction that causes an misaligned access for a

   a. word operation (2 byte) *mov [1003],ax*
   b. double operation (4 byte) *mov [1003],ax*

8. (3 pts) For an INTR interrupt on the 8088/8086, explain how the vector number gets generated.
   *The 8088/8086 generates two interrupt acknowledge bus cycles using the INT# output, in the 2nd cycle the interrupting devices places the interrupt vector number on the lower 8-data lines (D0-D7). The interrupt vector address is then the vector number * 4.*

9. (3 pts) How many bytes is each entry in the interrupt vector table of the 88/86 and what is stored in the entry?
   4 bytes; CS:IP

10. (3 pts) When a hardware interrupt is generated on the x88/x86, the current instruction is finished, and then some values are pushed on the stack before the Interrupt Service Routine is called. What is pushed on the stack?
    The CS:IP of the return address is pushed and the flag register is pushed.

11. (4 pts) What is the difference between POLLED IO and Interrupt-driven IO?

In Polled IO, the cpu continually checks the device to see if IO needs to be performed. In interrupt driven IO, the IO device uses a hardware interrupt to signal the processor that IO service is required.

12. (4 pts) What is the difference between a FIXED PRIORITY scheme and a ROTATING priority scheme for resolving simultaneous interrupts? Assume 8 interrupt sources (IRQ0 thru IRQ7).

For fixed priority the priority used for resolving simultaneous interrupts is never changed (if IRQ0 is the highest priority, it is always the highest priority). Rotating priority changes the priority after each interrupt so that each interrupt source has a chance at being the highest priority interrupt.

13. (3 pts) When an hardware interrupt is generated on the x86/x88, interrupts are disabled before the ISR routine is called. When would it be a good idea to re-enable interrupts within the ISR?

If the ISR is for a low priority interrupt, it should re-enable interrupts as soon as possible upon entry to the ISR so that higher priority interrupts can be serviced.

14. (3 pts) Given an example of a handshaking line on the parallel printer interface that we studied in class. Explain what it was used for.

The BUSY output of the printer was used to check to see if the printer was ready for new data. The STROBE input to the printer was used to indicate that valid data was present on the printers data lines.

15. (3 pts) What is a 'wait' state used for with a read/write cycle between a microprocessor and memory?

A wait state is used when interfacing a fast processor to a slow memory so that the memory has extra time to accept from the processor or provide data to the processor.

16. (3 pts) The 386+ used a 2T cycle for a read/write cycle instead of the 4T cycle that the 8088/8086 used. What does this mean?

2T means that the 386+ used two clock cycles for memory operations; the 88/86 used 4 clocks for a memory operation.

17. (3 pts) From a bus perspective, what control line on the 486 distinguishes a Memory operation (i.e, MOV ax, [1000h]) from an IO operation (generated by an IN or OUT instruction)

The M/IO# line distinguishes a memory operation from an IO operation.

18. (15 pts) Complete the code for an Interrupt Service Routine that reads a byte from port 200h and places it in a circular buffer. The *hea*d and *tail* offsets are initially set equal to 0. The CBUFF is the storage area used for the circular buffer, and MAXBYTES is the size of the buffer. The ISR should discard the input byte if it will cause the circular buffer to become full. If the input byte is discarded because of this, then set the STATUS word to any non-zero value.

REMEMBER that this is an INTERRUPT SERVICE ROUTINE!!!!!!!

```
        .stack  200h
        .data

DPORT       equ     200h
MAXBYTES    equ     512
CBUFF       db maxbytes dup (?)
HEAD        dw      0
TAIL        dw      0
STATUS      dw      0

        .code
;; put your code here
        push    ds                  ;save registers
        push    ax
        push    bx
        push    si
        push    dx
        mov     dx, DPORT           ;get data port number
        mov     bx, @data           ;get data segment
        mov     ds, bx
        mov     bx, [HEAD]          ; get head index
        inc     bx                  ;increment by one
        cmp     bx, MAXBYTES        ;check if wraparound
        jb      skip
        xor     bx,bx               ;reset equal to zero
skip:
        cmp     bx,[TAIL]           ;see if head = tail
        je      error               ; if equal, then overflow, exit
        in      al, dx              ;read port
        lea     si, CBUFF           ; get address of buffer
        mov     [si+bx],al          ;store byte in buffer at CBUFF+HEAD
        mov     [HEAD],bx           ;save head pointer
        jmp     exit
error:
        in      al,dx               ; read port to discard byte
        mov     ax,1
        mov     [status],ax         ; save '1' in status word
exit:
        pop     dx
        pop     si                  ;restore registers
        pop     bx
        pop     ax
        pop     dx
        iret                        ; use 'iret' instruction to return from interrupt
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