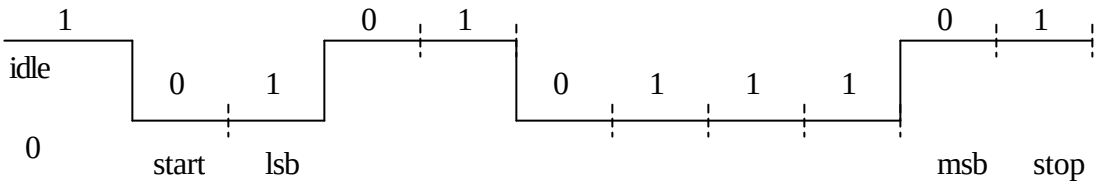
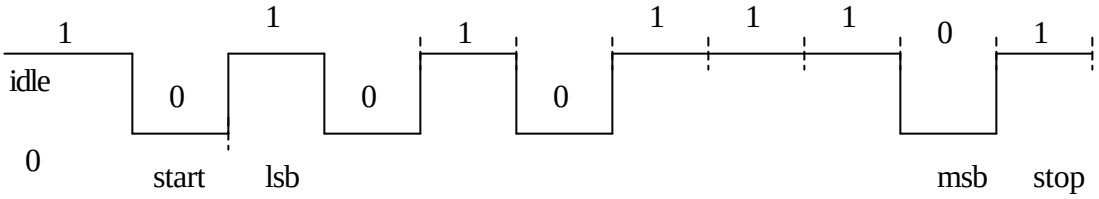
EE 3724 Test #4 Solutions - Summer '00 – Reese

1. (4 pts) The physical signaling on the USB ensures that a '0' is transmitted after every 6 consecutive '1's. Why is this needed?
   This forces a transition in the signal at least once every 7 bit times – this allows the receiver clock to remain synchronized to the bit stream.

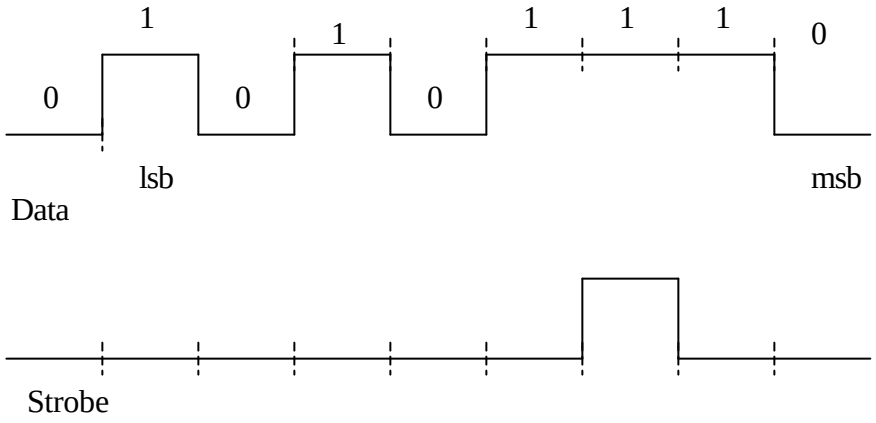
2. (4 pts) Draw the waveform for sending an 8 bit value of 75h using **NRZI** encoding as defined by the USB standard. Assume the idle state of the serial line is a '1' and that one start bit of '0' is used at the beginning of the transmission. End the transmission with returning the line to the idle state.



3. (4 pts) Draw the waveform for sending an 8 bit value of 75h using **NRZ** encoding(used by RS232). Assume the idle state of the serial line is a '1' and that one start bit of '0' is used at the beginning of the transmission. End the transmission with returning the line to the idle state.



4. (4 pts) Draw the waveform for sending an 8 bit value of 75h using **DATA STROBE** encoding. Assume the initial values of both data and strobe are '0'. Show the signaling for the 8-data bits only (no framing bits such as start/stop).



5. (4 pts) Why is differential signaling used in the USB standard?
For rejection of common mode noise.

6. (8 pts) Define the terms:
   a. half-duplex - *data transmitted in only one direction at a time*

   b. full-duplex. – *data transmitted in both directions at the same time.*

   c. What term applies to the RS-232 serial standard? *Full-duplex, has Tx/Rx wires in cable.*

   d. What term applies to the USB serial standard? *Half duplex; D+/D- wires transmit data in one direction during a data transfer.*

7. (3 pts) Which of the following is a system bus standard? (circle one)
   a. AGP
   b. PCI - Peripheral Component Bus
   c. SCSI
   d. USB
   e. DMA

   AGP is port between a graphics card and memory (is not a system bus); SCSI and USB are peripheral busses (out of the box busses), and DMA is a term that means Direct Memory Access.

8. (4 pts) Why was the Advanced Graphics Port invented?
   3D Graphics video cards require high bandwidth to main memory – better performance can be achieved if a dedicated port to main memory is used rather than the PCI bus.

9. (4 pts) What does bus mastering mean?
   A device other than the CPU controls the bus – most modern bus standards support bus mastering – with bus mastering any IO device on the bus can control the bus.

10. (4 pts) Assume that a 32-bit wide bus allows one data transfer per clock. What is a common trick for doubling the bus bandwidth without adding any more pins to the bus?
   Clocking data on both edges of the clock.

11. (3 pts) Which of the following functions WOULD NOT be found in a system chipset for a Pentium class processor? (circle one)
    a. DRAM controller
    b. Cache controller
    c. Floating point unit
    d. USB interface
    e. Video controller
    f. PCI interface

    The floating point unit will be on the Processor chip – all of the other items in the list can be found on chipsets (yes, even video controllers – we looked at the Intel 810 chipset and saw this).

12. (27 pts) Answer the following questions from a list of the following terms:
Horizontal_Sync_Frequency Vertical_Sync_Frequency Dot_Clk_Frequency
Split_Transaction Refresh_Rate Frame_Rate 2D_Graphics 3D_Graphics
Exponent_field Signifcand_Field NaN

a. Number of dots per horizontal line on screen
= (*Dot_clk_frequency*) divided by (*Horizontal Sync Freq*)

b. Rate at which screen is retraced by video controller: *Refresh_Rate*

c. Graphics capabilities mainly require fast block memory copies:
2D Graphics

d. Graphics capabilities require significant arithmetic processing and increased memory bandwidth by Video controller: *3D Graphics*

e. Increasing the size of this field in a floating point format increases the range of the floating point format: *exponent field*

f. Increasing the size of this field in a floating point format increases the precision of the floating point format: *significand field*

g. Number of horizontal lines on screen
= (*horizontal_sync*) divided by (*vertical_sync*)

h. Rate at which new 'scenes' are produced in computer animation:
Frame Rate

i. A 'special' number in the IEEE 754 floating point format: *NaN*

13. (5 pts) Convert the number -37.6875 to single precision floating point format:

Sign bit: 1 (negative)
Exponent field: ***10000100*** (84h) (8 bits)
Significand field: ***001011011*** 0……0 (23 bits)

37 = 25h = 00100101
.6875 * 2 = 1.375 (>= 1, so bit = 1)
.375 * 2 = 0.75 (< 1, so bit = 0)
.75 * 2 = 1.5 (>= 1, so bit = 1)
.5 * 1 = 1.0 (> = 1, so bit = 1)

0.6875 = 0.1011
37.6875 = 100101.1011 = 1.***001011011*** x 2^{5}

Exponent = 5 + 127(bias) = 132 = 84h = 10000100

14. (5 pts) Convert the following number in single precision floating point format to its decimal value (no exponents allowed in the final decimal value).

Sign bit: 0
Exponent field: 01111110
Significand Field: 0100 0000 0000 ……0

Sign is positive
Exponent field = 7Eh, so exponent = 7Eh – 127 = 126 – 127 = -1
Number = 1.01×2^{-1} = 0.101 b = 0.5 + 0.125 = ***+0.625***

15. (4 pts) Explain what the SIMD Floating point extensions are on the Pentium III. Give the new register sizes, and explain how they are used.
The new registers are 128 bits in length, and are divided into 32-bit fields. This gives 4 single precision floating point numbers or 4 integers. The new instructions allow the same operation to be applied to all four fields, which provides 4 floating point ops or scalar ops in one instruction.

16. (9 pts) A new arithmetic mode called Saturating addition was added with the MMX instructions. Compute the following sums below:
    a. F0h + 11h (unsigned, saturated mode): *result will overflow unsigned, so final result is FFh.*

    b. 83h + F0h (signed, saturated mode): *result will overflow signed on the negative end (smaller number than 80H), so result is clamped to 80h.*

    c. 7F + Feh (signed, saturated mode*)* *No overflow, so result is just the sum of these two numbers, or 7Dh.*

17. (4 pts) When the term 'bus' is applied something like the USB, it has a distinct meaning. What operations/features constitute a bus?
A bus has multiple devices connected to it, and any transaction on the bus is seen by all devices connected to the bus.

18. (4 pts). The USB supports a data transfer operation called an *Interrupt transfer*. In class, we discussed why this was not a TRUE interrupt. Explain what the interrupt transfer is on the USB and how it differs from a true interrupt.
*A true interrupt has the interrupting device initiate the interrupt at ANY time. On the USB bus, the controller **reserves** a small period of time during each frame (1 frame = 1ms) for a device to send an interrupt request packet. The device can only use this reserved bus time to indicate that it has an interrupt. If the controller receives an interrupt request packet, then the device is serviced in the next frame.*