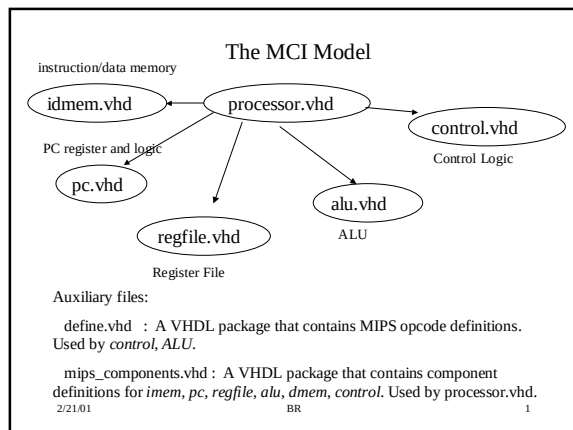




- ### Changes between SCI and MCI models
- All additional muxes/registers have been placed in *processor.vhd* model.
 - One model for both instruction and data memory
 - After *.obj* file has been produced from an assembly source file (.s) by *spim2obj.pl* utility, must hand edit the file to initialize any data contents.
 - Two processes uses in *control.vhd* to represent the finite state machine.
 - Process 'stateproc' represents DFFs of state machine (do not edit this process)
 - Process 'main' represents the combinational logic of the state machine (basically just a case statement)
 - You will need to make the same pathname changes to 'mci.mpf' as you did for 'sci.mpf' after unzipping the archive file.
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More on *control.vhd*

States are represented by names in a typedef statement:

```

type mystate is (FETCH, DECODE, RTYPE_A, RTYPE_B,
                 ITYPE_A, ITYPE_B, BRANCH_A,
                 JUMP_A, MEMORY_A, MEMORY_B,
                 MEMORY_C);
  
```

These states correspond to numbered states in the book – I added the 'ITYPE_A' and 'ITYPE_B' states to handle immediate instructions.

To support other instructions, you may need to add new states, and corresponding code in the case statement with the 'main' process.

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External Assignment

- The control.vhd file only implements instructions addi, add, beq, jmp, lw
- Add support for instructions bne, sw, and, andi, or, ori, sub, slt, slti
 - An assembly test program will be provided later that can be used as an 'acid' test for your changes to the MCI model. You can also write your own test for these changes.
 - You will only need to modify 'control.vhd' to support these instructions.
- For an extra challenge, try adding support for 'jr'. You will have to modify more than 'control.vhd'!!!

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