

Register file normally has 1 write port + 2 read ports.

Why? `add r2, r4, r5` is `r2 = r4 + r5`.

The diagram shows a central box labeled "REGISTER FILE 32 x 32". On the left, there are two input ports: "write_address[4:0]" and "write_data[31:0]". On the right, there are two output ports: "read_data_a[31:0]" and "read_data_b[31:0]". On the left side of the box, there are two input ports: "rd_address_a[4:0]" and "rd_address_b[4:0]". Below the box, it says "32 locations x 32 bits."

Can be reading writing one operand while reading two others...

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Can we add more ports to register file? Yes...

The diagram shows a central box labeled "REGISTER FILE 32 x 32". On the left, there are four input ports: "write_addr_x[4:0]", "write_data_x[31:0]", "write_addr_y[4:0]", and "write_data_y[31:0]". On the right, there are four output ports: "read_data_a[31:0]", "read_data_b[31:0]", "read_data_c[31:0]", and "read_data_d[31:0]". On the left side of the box, there are four input ports: "rd_addr_a[4:0]", "rd_addr_b[4:0]", "rd_addr_c[4:0]", and "rd_addr_d[4:0]". To the right of the box, it says "RF is 32 locations x 32 bits. 2 write ports, 4 read ports".

Why add more ports?
If I want to execute MORE THAN one instruction per clock need to fetch 2 read operands for each instruction, complete a write for each instruction operand.

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Multi-Ported Register File Design has Limits

- Area of the register file grows approximately with the square of the number of ports
⇒ Typically routing limited, each new port requires adding new routing in both X and Y direction

The diagram compares two routing schemes. On the left, labeled "1 write Port 2 Read Ports", it shows a grid with 2 horizontal blue lines (Read1A, Read1B) and 1 vertical green line (Write1). On the right, labeled "2 write Ports 4 Read Ports", it shows a grid with 4 horizontal blue lines (Read1A, Read1B, Read2A, Read2B) and 2 vertical green lines (Write1, Write2). The grid is composed of "Bit Cell" units. Below the grids, the output ports are labeled: "Dout1A", "Dout1B" for the first grid, and "Dout2A", "Dout2B", "Dout1A", "Dout1B" for the second grid.

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Multiported Register Files (cont)

- Read Access time of a register file grows approximately linearly with the number of ports
 - ⇒ Internal Bit Cell loading becomes larger
 - ⇒ Larger area of register file causes longer wire delays
- What is reasonable today in terms of number of ports?
 - ⇒ Changes with technology, 15-20 ports is currently about the maximum (read ports + write ports)
 - ⇒ Will support 5-7 execution units simultaneous operand accesses from register file

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