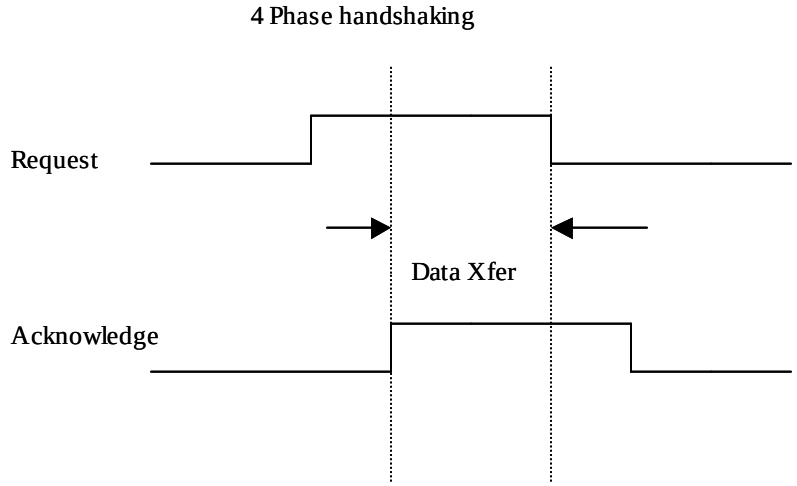
Computer Architecture: Spring 2001 – Test 4 Solutions - Input/Output

1. (9 pts) a. Define throughput and latency.
   b. Given a fixed bus bandwidth, if I increase throughput, what happens to latency? Increases or Decreases?

Latency is the time from when the operation is started to when the operation is finished. Throughput is number of operations per unit time. For fixed bandwidth, if throughput is increased, then latency is increased.

2. (6 pts) What basic control lines are needed for a central arbitration scheme? Explain their function.
   Bus Request : asserted by a device that is requesting the bus
   Bus Grant: asserted by arbiter to grant the bus to a device

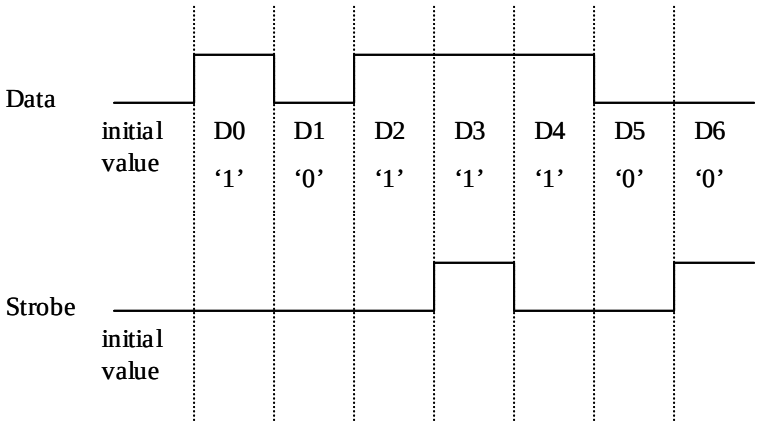
3. (4 pts) Show the 4 phase handshaking protocol discussed in class for an asynchronous data transfer. *See notes.*



(4 pts) What is the function of the latency timer on the PCI bus? Why is it a good idea to have this timer?
The latency timer limts the amount of time a master can control the bus. This reduces the arbitration latency for other devices needing the bus.

4. (5 pts) IEEE Firewire uses data strobe encoding for data transmission. Show this encoding for the 7 bit data transmission 0011101. Send the data LSB first. Assume data and strobe lines are initially '0'.

0011101 Send LSB first, Data Strobe Encoding

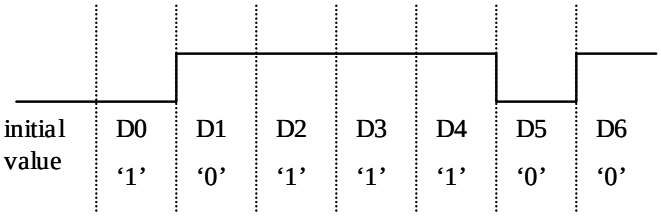


5. (3 pts) Show how a clock signal can be extracted from the data/strobe encoding used in IEEE Firewire.

   See Notes --- the clock signal is the exclusive OR of the data and strobe signals.

6. (6 pts) a. Show the NRZI encoding used by USB is used to send the data value 0011101. Send the data LSB first.
   b. How does USB maintain data synchronization?

0011101 Send LSB first, NRZI encoding



7. (4 pts) Why is differential data signaling used for both USB and Firewire?
   To reduce common node noise.

(4 pts) What is a 'turnaround' cycle on a PCI bus?
Many lines on the PCI bus can be driven by multiple devices. A turnaround cycle is a clock cycle which allows the one device to turn off its drivers and another device to turn on its drivers (the Address/Data bus needs a turnaround cycle between the master providing the address and the target providing the data).

8. (4 pts) Newer versions of the SCSI bus and RAMBUS both use advanced electrical signaling to increase bus bandwidth. Discuss one of these signal methods and explain why it is faster.

   Both standards used limited swing voltage signaling that is approximately +/- 200 mv. Signaling is faster because of less voltage swing. SCSI uses differential signaling, while RAMBUS uses single-ended signaling.

9. (6 pts) Assume the shared bus cache consistency protocol discussed in class. If processor 1 has block 'A' in the exclusive clean state, and processor 2 experiences a 'read miss' to block 'A', what happens? What states does block A end up with in both caches?

   Both processors end up with Block A in the shared clean state.

10. (6 pts) Assume the shared bus cache consistency protocol discussed in class. If processor 1 has block 'A' in the exclusive clean state, and processor 2 experiences a 'write miss' to block 'A', what happens? What states does block A end up with in both caches?

    Processor 1 ends up with block A being invalid, Processor 2 has block A as exclusive modified.

11. (4 pts) What is seek time in a fixed disk? What is rotational latency?

    Seek time is the time required to position the head over the correct track. Rotational latency is the time required for the correct sector to rotate under the head.

12. (4 pts) How does RAID increase data *availability* in a disk IO system? How does RAID increase data *reliability* in a disk IO system?

    Data availability is increased due to redundancy of data storage, either via parity bits or mirroring. This allows hot swapping which means that a single failed disk can be replaced without taking down the entire array.

    Data reliability is increased due to the detection of errors via the Parity bits.

    Performance is increased via parallel access to multiple disks.

(5 pts) The SCSI bus supports *split transactions*. Explain this term and discuss why this increases throughput in a disk IO system.

Split transaction means to send the address information of a transaction, and then allow other operations on the bus before completing the data portion of the first tranaction. For disks, this means to send the seek command to a disk, then access other disks before coming back and retrieving the data from the first seek command.

13. (6 pts) What is the difference between a VLIW and a Superscalar architecture? How are they the same?
    Both architectures execute instructions in parallel to achieve a CPI < 1.0. A VLIW architecture uses static scheduling of instructions (relies on compiler to solve most hazards) while a Superscalar architecture uses dynamic instruction scheduling (hardware solves all hazards).

14. (4 pts) What is a Vector operation? Give an example.

    A vector operation is the same operation applied to multiple sets of data. The Pentium 4 allows a floating point operation to be applied to 4 single precision FP numbers (each 32 bits) that are contained in a 128 bit registers.

15. (4 pts) Give at least two specific reasons why the PCI bus can't reach its peak I/O transfer rate.
    Multiplexed address/data bus, turnaround cycles, handoff cycles between masters.

16. (4 pts) Is the Transmeta CPU discussed in class a VLIW or Superscalar architecture? How does the Transmeta CPU support X86 legacy code streams?

    The Transmeta CPU is a VLIW architecture and uses dynamic translation of X86 instructions to native VLIW code.

17. (4 pts) When do signal reflections on a bus become an issue? What are ways in which reflections on a bus can be reduced?

    When travel time of a signal (propagation delay from start to end of a wire) becomes much greater than the rise/fall time of the signal, reflections can corrupt the signal. Signal termination schemes (either active or passive) can be used to damp reflections.

18. (4 pts) Discuss some other method other than central arbitration for allowing multiple bus masters.

    Carrier Sense Multiple Access (Ethernet), time division multiplexing, hardware daisy chain arbitration, token ring are all methods for allowing multiple bus masters.