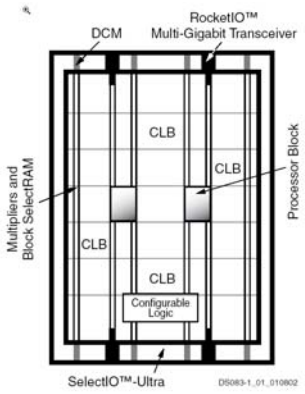
Programmable System-on-a-Chip (PSoC)

- CPU core + programmable logic
- PSoCs becoming more important because NRE (non-recoverable engineering) costs keep rising as we go deeper into sub-micron and nanometer technologies
  - NRE cost is the cost of the first chip
  - A mask set is used to pattern layers/materials (metal, polysilicon, diffusion, etc) on wafer
  - Masks are becoming increasingly expensive
  - The higher the NRE, the more chips you have to sell to recover costs
- A programmable chip can be used in more applications, so more potential customers!!!

Xilinx Pro FPGA

Has PowerPC CPU cores, Xilinx VirtexII programmable logic

RocketIO supports high-speed serial IO such as 10Gb ethernet



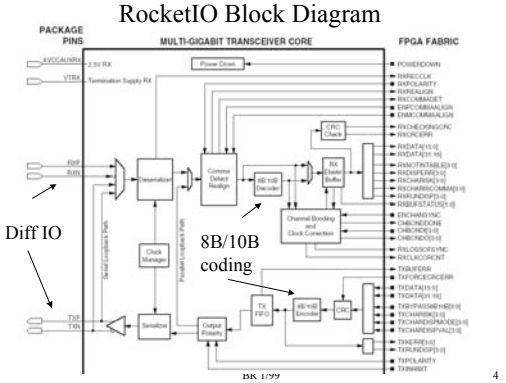
Supported Standards via RocketIO

Table 1: **Protocols Supported by RocketIO Transceiver**

Protocol	Channels (Lanes)	I/O Baud Rate (Gb/s)	Reference Clock Rate (MHz)
Fibre Channel	1	1.06	53
		2.12	106
		3.1875 (1)	159.375
Gigabit Ethernet	1	1.25	62.5
10Gbit Ethernet	4	3.125	156.25
Infiniband	1, 4, 12	2.5	125
Aurora	1, 2, 3, 4, ...	0.840 – 3.125	42.00 – 156.25
Custom Protocol	1, 2, 3, 4, ...	up to 3.125	up to 156.25

These are all Serial IO standards

RocketIO Block Diagram



Coding for Serial Data Transmission

- Want to distinguish start/end of packets
- Want a certain number of signal transitions per unit time (transition density) so that receiver clock can remain synchronized to bit stream
- Want to be able to detect transmission errors.

8B/10B Coding

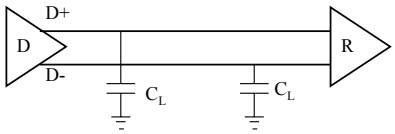
- 8B/10B coding means that 10 bits are used to encode 256 (8-bit) data characters.
  - 10 bits give 1024 combinations, why the extra bits?
- Data sent in packets that is formatted as header (start of packet), packet data, end of packet
  - Need special control characters (K-characters) that will be used for start/end of packet designation, sync character, other control
  - Extra bits used to encode K-characters (12 in 8B/10B code)
  - Data is called D-characters
  - A subset (called commas) of the K-characters has bit encoding which is guaranteed to NEVER appear in the serialized stream of D-characters.

8B/10B Coding (cont)

- Code is run length limited (RLL) – guarantees no more than five consecutive '1's or five consecutive '0's
  - Guaranteed transition density (transitions per unit time).
  - Allows receiver clock PLL to remain synchronized to input data stream
- *Disparity* – difference in number of received '1's and '0's in a serial stream over some length.
  - +1 disparity (one more '1' than '0')
  - -1 disparity (one more '0' than '1')
- Code is *DC-balanced* if equal numbers of '1's and '0's is sent.

LVDS

- LVDS – low voltage, differential signaling
  - Two lines: D+, D-
  - Signal swing is 300 mv, typically about 1.25V



For long lines, CL can be significant. If lines are quiescent (unchanging, high disparity) for a long period of time, charge builds up on CL. The energy in a single bit transition may not be enough to overcome this stored charge.

Disparity/DC-balance, and LVDS

- If a code has low disparity (low difference in number of '0's, '1's sent) then charge does not get chance to build up.
- For a given period of time, if equal numbers of '1's, '0's is sent, this is 0 disparity. This transmission is said to be 'DC-balanced'.
- Each 10-bit symbols in the 8B/10B code either has a disparity of 0, +2 (six ones, four zeros), or –2 (four ones, six zeros)
- *Running Disparity* is the disparity for a given sequence of symbols, e.g. a packet
  - Disparity for a in a 10G ethernet packet is guaranteed to be either +1 or –1.

Error Detection

- CRC (Cyclic Redundancy Check) – much more complicated than a XOR checksum, much more robust in detecting errors
  - 32-bit CRC supported in RocketIO logic
- Running disparity can also be used to detect an error.

RocketIO Physical Interface

Table 4-1: **Differential Transmitter Parameters**

Parameter		Min	Typ	Max	Units	Conditions
V_{OUT}	Serial output differential peak to peak (TXP/TXN)	800		1600	mV	Output differential voltage is programmable
V_{TTX}	Output termination voltage supply	1.8		2.8	V	
V_{TCM}	Common mode output voltage range	1.5		2.5	V	
V_{SKEW}	Differential output skew			15	ps	

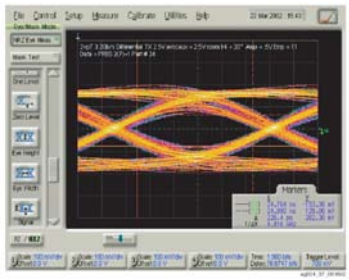
This is not LVDS standard as minimum differential is 800 mV.

Note large common-mode range.

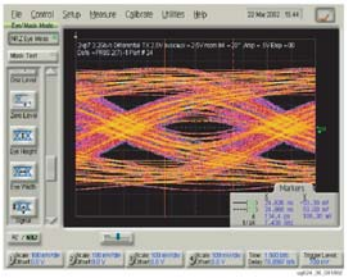
Eye Diagram

- An EYE diagram used to measure quality of transmission channel.
- Generate pusedo-random data over channel, feed received data into vertical channel of scope
- Feed data rate (received generated clock) into horizontal sweep.
- An 'open' eye corresponds to minimal distortion.
- A closed eye shows signal *jitter*.
  - *Jitter* is short term variations of a signal from its ideal position in time.
  - Jitter caused by intersymbol interence, power supply noise, transmission channel loss, etc.

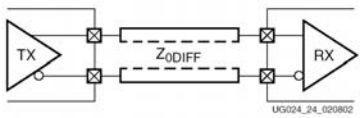
Open Eye



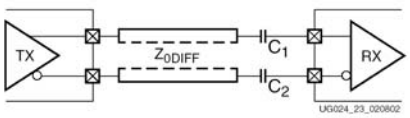
Closed Eye



Connecting High Speed Serial Links



DC coupling – possible if same common voltages used.



Used if incompatible common-mode voltages or optical link is used. For AC coupling, *DC-balance* is very important because can't transmit signal with DC-content.

PowerPC 405-D Core

- Thirty-two 32-bit registers
- Load/Store instruction set
  - Multiply accumulate
  - Three timers
  - 64-bit time base for timers
- 16KB Icache, 16KB Dcache
- 5-stage pipeline (average of about 1 clock per instruction)
- Memory Management Unit (MMU) so can execute virtual memory Operating System (OS).
- No hardware floating point
- Operation at 300+ Mhz

PowerPC 405 Block Diagram

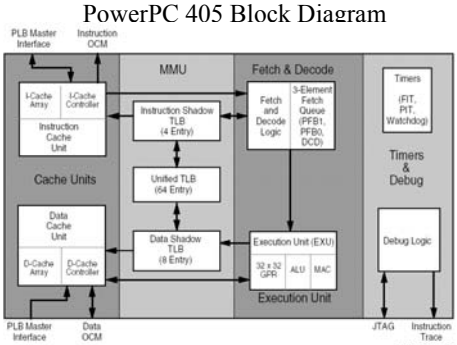


Figure 7: **Embedded PPC405 Core Block Diagram**

PowerPC core to FPGA connection

FPGA cells

DCR = Device Control Register Bus

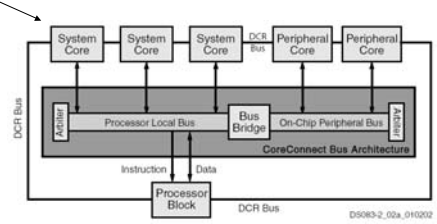
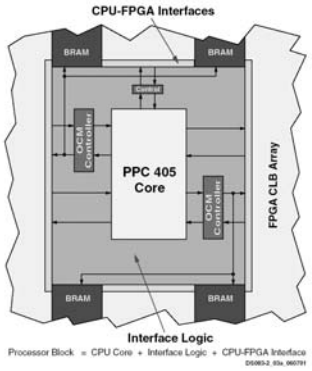


Figure 6: **CoreConnect Block Diagram**

Access to Memory Outside of Caches



OCM – on chip memory controller

BRAM – block RAM in FPGA logic.

Virtext-II FPGA Resources

- 18x18 2's-complement multiplier
- 18Kb Dual Port SRAM blocks that can configured as shown below

Table 17: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

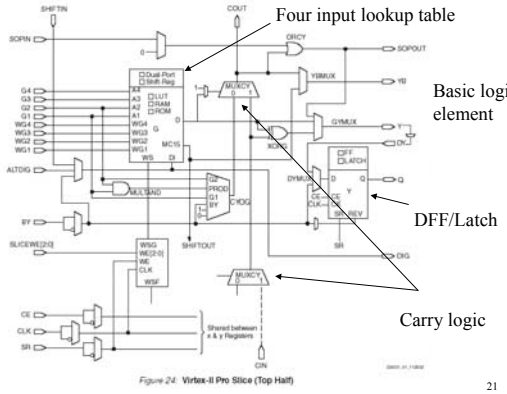


Figure 24: **Virtex-II Pro Slice (Top Half)**

Cypress Microsystems PSOC

- Programmable System on a Chip
- 8-bit Microcontroller (CPU clock up to 24 Mhz)
- Programmable logic that supports both digital and analog logic
- Programmable Digital Blocks
  - Pulse width modulators
  - Timers/Counters
  - UARTs/SPI blocks
- Programmable Analog Blocks
  - A/D conversion
  - Analog compartor
  - Temperature sensor
  - Analog Modulator
  - Sinewave waveform Generation

Sample Blocks

Analog to Digital Converters
ADC Incremental 12 Bit
ADC Incremental Variable Resolution 7 to 13 Bit
ADC Delta Sigma 8 Bit
ADC Delta Sigma 11 Bit
ADC True Dual Incremental Variable Resolution 7 to 13 Bit
ADC SAR (Successive Approximation Register) 6 Bit
ADC True Triple Incremental Variable Resolution 7 to 13 Bit
Amplifiers
Inverting Programmable Gain
Comparator
Instrumentation Amplifier
Non-Inverting Programmable Gain
Analog Communications
DTMF Dialer
Counters
Counter 8 Bit
Counter 16 Bit
Counter 24 Bit
Counter 32 Bit

Digital to Analog Converters
DAC 6 Bit (True DAC)
DAC 8 Bit (True DAC)
DAC 9 Bit (True DAC)
Multiplying DAC 6 Bit
Multiplying DAC 8 Bit
Digital Communications
CRC Generator 16 Bit (Cyclical Redundancy Check)
I2C Master
I2C Slave
IrDA Optical Transmitter
IrDA Optical Receiver
Serial Receiver 8 Bit
SPI Master (Serial Peripheral Interconnect)
SPI Slave
Serial Transmitter 8 Bit
UART (Universal Asynchronous Receiver Transmitter)
Filters
Band-Pass Filter
Low-Pass Filter (Bessel, Butterworth, Chebyshev, Elliptical)
Generics
Switched Cap Analog Block

Wide range of building blocks available as library elements from within design tool supplied by Cypress.

CPU

- 8-bit CPU, close to a 6502 core (same core used in the Apple II and original Nintendo)
- 8-bit Accumulator (A), 8-bit Index Register (X), 16-bit Program counter, 8-bit flag register, 8-bit stack pointer register
  - 6502 also had another index register (Y) that is missing in this core.
- Two register banks of 256 locations each
  - Used for RAM, also for control registers of onboard peripherals
- Non-pipelined core, all operations take at least 5 clocks, most 6 or 7 clocks, some take up to 13 clocks

Programmable System-on-a-Chip

- The Xilinx-II Pro and Cypress PSOC are two examples are programmable system-on-a-chip
- Processor core + programmable Logic is a powerful combination.
- Xilinx device intended for high-end, high-performance applications
- Cypress device for low-end, low-cost.