Topics for Final (Wed Dec 13th, 8:00)

- Technology Scaling
  - power, area, delay
- Timing Models
  - RC, Lookup Table, Logical Effort
- Timing optimization
  - logic effort, Tilos algorithm
- Dynamic Logic
  - DCVSL
  - Domino Gates, Pipelined systems using Domino
- Memories
  - Static RAM architecture (decoding, cell design)
- Standard Cell library design
  - Template design, tool methodology