CY7C4421/4201/4211/4221
CY7C4231/4241/4251

64/256/512/1K/2K/4K/8K x 9 Synchronous FIFOs

Features

- **High-speed, low-power, First-In, First-Out (FIFO) memories**
  - **64 × 9 (CY7C4421)**
  - **256 × 9 (CY7C4201)**
  - **512 × 9 (CY7C4211)**
  - **1K × 9 (CY7C4221)**
  - **2K × 9 (CY7C4231)**
  - **4K × 9 (CY7C4241)**
  - **8K × 9 (CY7C4251)**
- **High-speed 100-MHz operation (10 ns Read/Write cycle time)**
- **Low power (I_{CC} = 35 mA)**
- **Fully asynchronous and simultaneous Read and Write operation**
- **Empty, Full, and Programmable Almost Empty and Almost Full status flags**
- **TTL-compatible**
- **Expandable in width**
- **Output Enable (OE) pin**
- **Independent Read and Write enable pins**
- **Center power and ground pins for reduced noise**
- **Width-expansion capability**
- **Space saving 7 mm × 7 mm 32-pin TQFP**
- **32-pin PLCC**
- **Pin-compatible and functionally equivalent to IDT72421, 72201, 72211, 72221, 72231, and 72241**

Functional Description

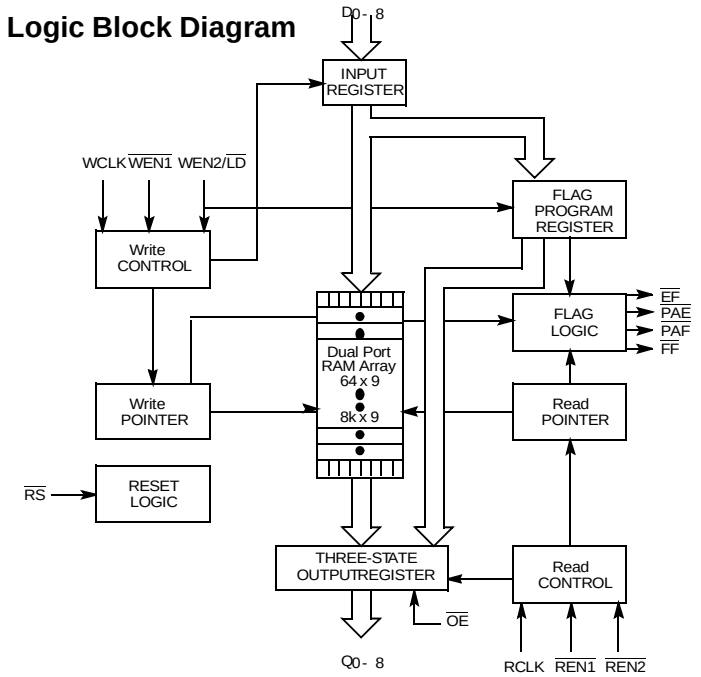
The CY7C42X1 are high-speed, low-power FIFO memories with clocked Read and Write interfaces. All are 9 bits wide. The CY7C42X1 are pin-compatible to IDT722X1. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two Write-enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running Read clock (RCLK) and two Read-enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C42X1 has an output enable pin ($\overline{OE}$). The Read (RCLK) and Write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous Read/Write applications. Clock frequencies up to 100 MHz are achievable.

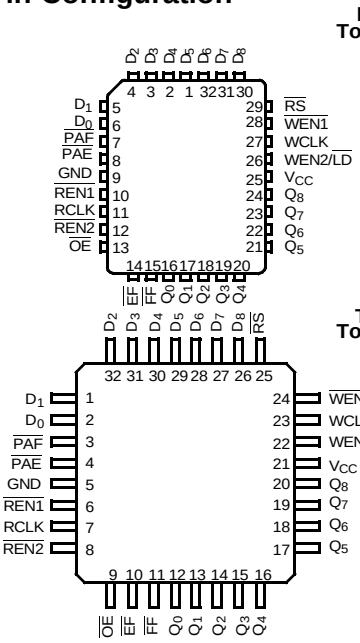
Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram



Pin Configuration

PLCC Top View



TQFP Top View

Selection Guide

		-10	-15	-25	Unit
Maximum Frequency		100	66.7	40	MHz
Maximum Access Time		8	10	15	ns
Minimum Cycle Time		10	15	25	ns
Minimum Data or Enable Set-up		3	4	6	ns
Minimum Data or Enable Hold		0.5	1	1	ns
Maximum Flag Delay		8	10	15	ns
Active Power Supply Current	Commercial	35	35	35	**ICC1**
	Industrial	40	40	40	

	CY7C4421	CY7C4201	CY7C4211	CY7C4221	CY7C4231	CY7C4241	CY7C4251
Density	64 × 9	256 × 9	512 × 9	1K × 9	2K × 9	4K × 9	8K × 9

Functional Description

The CY7C42X1 provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty – 7 and Full – 7.

The flags are synchronous, i.e., they change state relative to either the Read clock (RCLK) or the Write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full, and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle.

All configurations are fabricated using advanced 0.65µ N-Well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Architecture

The CY7C42X1 consists of an array of 64 to 8K words of 9 bits each (implemented by a dual-port array of SRAM cells), a Read pointer, a Write pointer, control signals (RCLK, WCLK, REN1, REN2, $\overline{WEN1}$, WEN2, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{FF}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs ($Q_{0–8}$) go LOW t_{RSF} after the rising edge of $\overline{RS}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or Write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

FIFO Operation

When the $\overline{WEN1}$ signal is active LOW and WEN2 is active HIGH, data present on the $D_{0–8}$ pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the REN1 and $\overline{REN2}$ signals are active LOW, data in the FIFO memory will be presented on the $Q_{0–8}$ outputs. New data will be presented on each rising edge of RCLK while REN1 and $\overline{REN2}$ are active. $\overline{REN1}$ and $\overline{REN2}$ must set up t_{ENS} before RCLK for it to be a valid Read function. $\overline{WEN1}$ and WEN2 must occur t_{ENS} before WCLK for it to be a valid Write function.

An output enable ($\overline{OE}$) pin is provided to three-state the $Q_{0–8}$ outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the $Q_{0–8}$ outputs after t_{OE}.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid Read on its $Q_{0–8}$ outputs even after additional reads occur.

Write Enable 1 ($\overline{WEN1}$). If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only Write enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write clock (WCLK). Data is stored is the RAM array sequentially and independently of any on-going Read operation.

Write Enable 2/Load (WEN2/$\overline{LD}$). This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two Write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set active HIGH at Reset ($\overline{RS}$ = LOW), this pin operates as a second Write enable pin.

If the FIFO is configured to have two Write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going Read operation.

Programming

When WEN2/$\overline{LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/LD and WEN1 are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/LD and WEN1 are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/LD and WEN1 are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/LD input HIGH, the FIFO is returned to normal Read and Write operation. The next time WEN2/LD is brought LOW, a Write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/LD is LOW and both REN1 and REN2 are LOW. LOW-to-HIGH transitions of RCLK Read register contents to the data outputs. Writes and reads should not be preformed simultaneously on the offset registers.

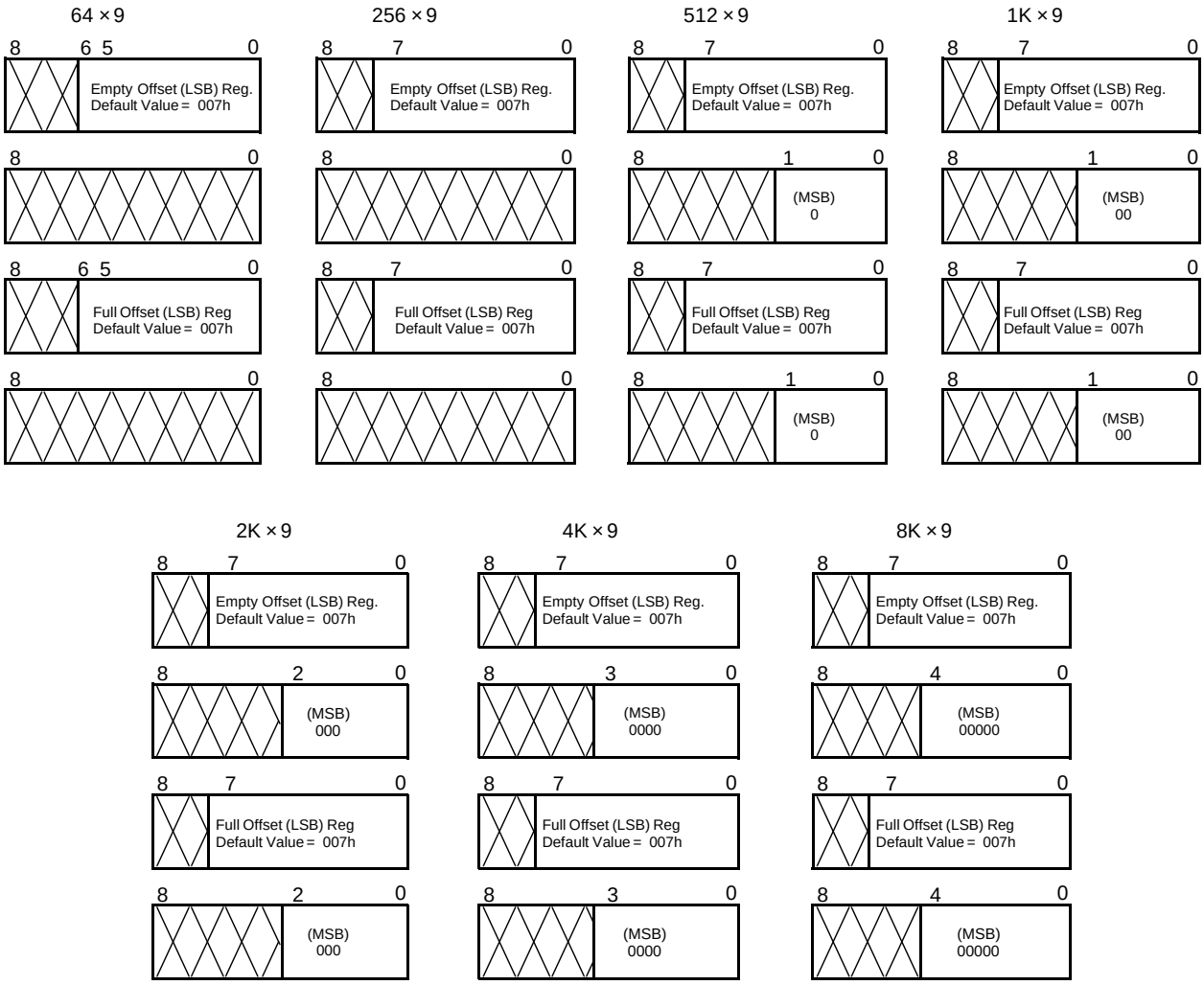


Figure 1. Offset Register Location and Default Values

Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the Read and Write pointers.

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n + 1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4421. (64 – m), CY7C4201 (256 – m), CY7C4211 (512 – m), CY7C4221 (1K – m), CY7C4231 (2K – m), CY7C4241 (4K – m), and CY7C4251 (8K – m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 1. Writing the Offset Registers

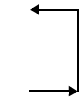
LD	WEN	WCLK[1]	Selection
0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB) 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Table 2. Status Flags

Number of Words in FIFO						
CY7C4421	CY7C4201	CY7C4211	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[2]	1 to n[2]	1 to n[2]	H	H	L	H
(n + 1) to 32	(n + 1) to 128	(n + 1) to 256	H	H	H	H
33 to (64 – (m + 1))	129 to (256 – (m + 1))	257 to (512 – (m + 1))	H	H	H	H
(64 – m)[3] to 63	(256 – m)[3] to 255	(512 – m)[3] to 511	H	L	H	H
64	256	512	L	L	H	H

Number of Words in FIFO							
CY7C4221	CY7C4231	CY7C4241	CY7C4251	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	H	H	L	L
1 to n[2]	1 to n[2]	1 to n[2]	1 to n[2]	H	H	L	H
(n + 1) to 512	(n + 1) to 1024	(n + 1) to 2048	(n + 1) to 4096	H	H	H	H
513 to (1024 – (m + 1))	1025 to (2048 – (m + 1))	2049 to (4096 – (m + 1))	4097 to (8192 – (m + 1))	H	H	H	H
(1024 – m)[3] to 1023	(2048 – m)[3] to 2047	(4096 – m)[3] to 4095	(8192 – m)[3] to 8191	H	L	H	H
1024	2048	4096	8192	L	L	H	H

Notes:
1. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a Read is performed on the LOW-to-HIGH transition of RCLK.
2. n = Empty Offset (n = 7 default value).
3. m = Full Offset (m = 7 default value).

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See *Figure 2*). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C42X1 devices provide four flag pins to indicate the condition of the FIFO contents. Empty, Full, $\overline{PAE}$, and $\overline{PAF}$ are synchronous.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN1}$ and WEN2/$\overline{LD}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

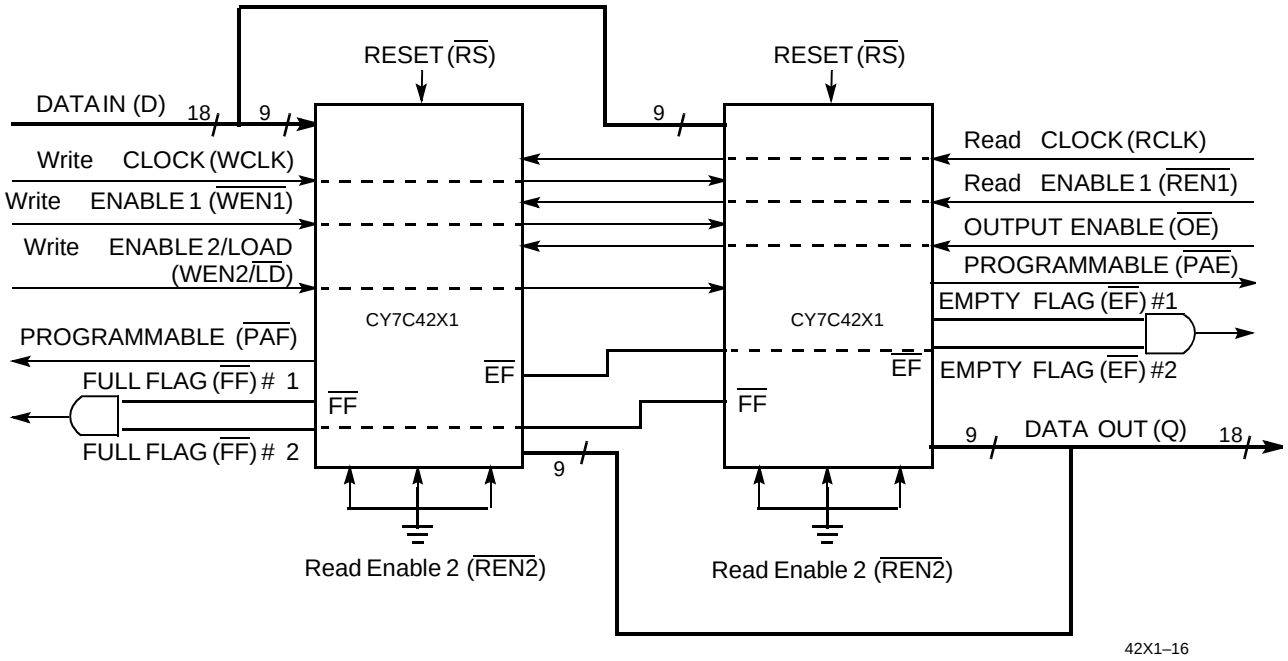


Figure 2. Block Diagram of 64 x 9, 256 x 9, 512 x 9, 1024 x 9, 2048 x 9, 4096 x 9, 8192 x 9 Synchronous FIFO Memory Used in a Width Expansion Configuration

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State..... –0.5V to +7.0V

DC Input Voltage..... –3.0V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[4]	–40°C to +85°C	5V ±10%

Pin Definitions

Pin	Name	I/O	Description
$D_{0–8}$	Data Inputs	I	Data Inputs for 9-bit Bus
$Q_{0–8}$	Data Outputs	O	Data Outputs for 9-bit Bus
WEN1	Write Enable 1	I	The only Write enable to have programmable flags when device is configured. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is HIGH. If the FIFO is configured to have two Write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ and $\overline{FF}$ are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2	I	If HIGH at reset, this pin operates as a second Write enable. If LOW at reset, this pin operates as a control to Write or Read the programmable flag offsets. $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
	Load	I	
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	Enables Device for Read Operation
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW, WEN2/$\overline{LD}$ is HIGH, and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial Read or Write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High-Z (high-impedance) state.

Note:
4. T_A is the "instant on" case temperature.

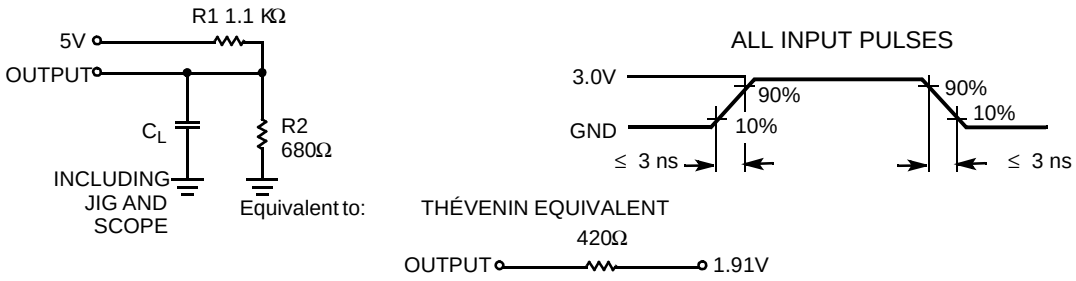
Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			–3.0	0.8	–3.0	0.8	–3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	–10	+10	µA
I_{OS}[6]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–90		–90		–90		mA
I_{OZL} I_{OZH}	Output OFF, High-Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	mA
I_{CC1}[7]	Active Power Supply Current		Commercial		35		35		35	mA
			Industrial		40		40		40	mA
I_{CC2}[8]	Average Standby Current		Commercial		10		10		10	mA
			Industrial		15		15		15	mA

Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[10, 11]



Switching Characteristics Over the Operating Range

Parameter	Description	-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_S	Clock Cycle Frequency		100		66.7		40	MHz
t_A	Data Access Time	2	8	2	10	2	15	ns
t_{CLK}	Clock Cycle Time	10		15		25		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		ns
t_{DS}	Data Set-up Time	3		4		6		ns

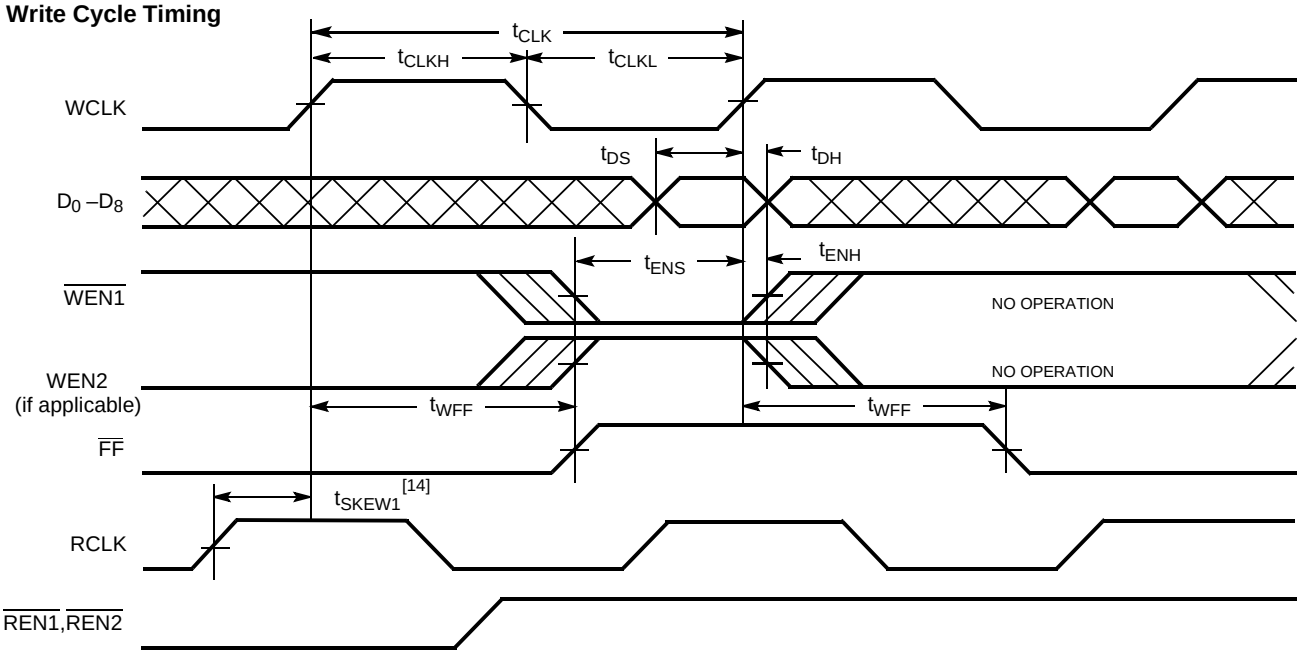
Notes:
5. See the last page of this specification for Group A subgroup testing information.
6. Test no more than one output at a time for not more than one second.
7. Outputs open. Tested at Frequency = 20 MHz.
8. All inputs = V_{CC} – 0.2V, except WCLK and RCLK, which are switching at 20 MHz.
9. Tested initially and after any design or process changes that may affect these parameters.
10. C_L = 30 pF for all AC parameters except for t_{OHZ}.
11. C_L = 5 pF for t_{OHZ}.

Switching Characteristics Over the Operating Range

Parameter	Description	-10		-15		-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{DH}	Data Hold Time	0.5		1		1		ns
t_{ENS}	Enable Set-up Time	3		4		6		ns
t_{ENH}	Enable Hold Time	0.5		1		1		ns
t_{RS}	Reset Pulse Width[12]	10		15		25		ns
t_{RSS}	Reset Set-up Time	8		10		15		ns
t_{RSR}	Reset Recovery Time	8		10		15		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25	ns
t_{OLZ}	Output Enable to Output in Low-Z[13]	0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	ns
t_{OHZ}	Output Enable to Output in High-Z[13]	3	7	3	8	3	12	ns
t_{WFF}	Write Clock to Full Flag		8		10		15	ns
t_{REF}	Read Clock to Empty Flag		8		10		15	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5		6		10		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	10		15		18		ns

Switching Waveforms

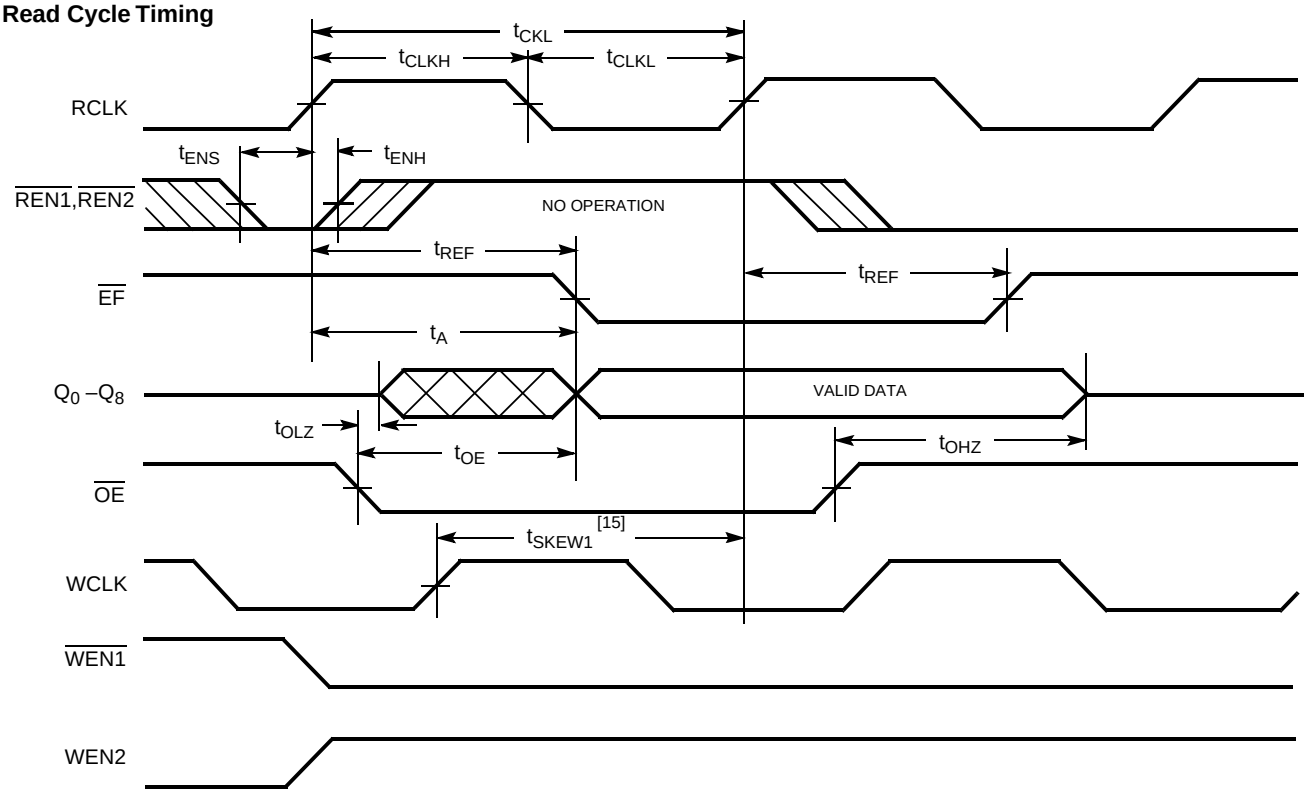
Write Cycle Timing



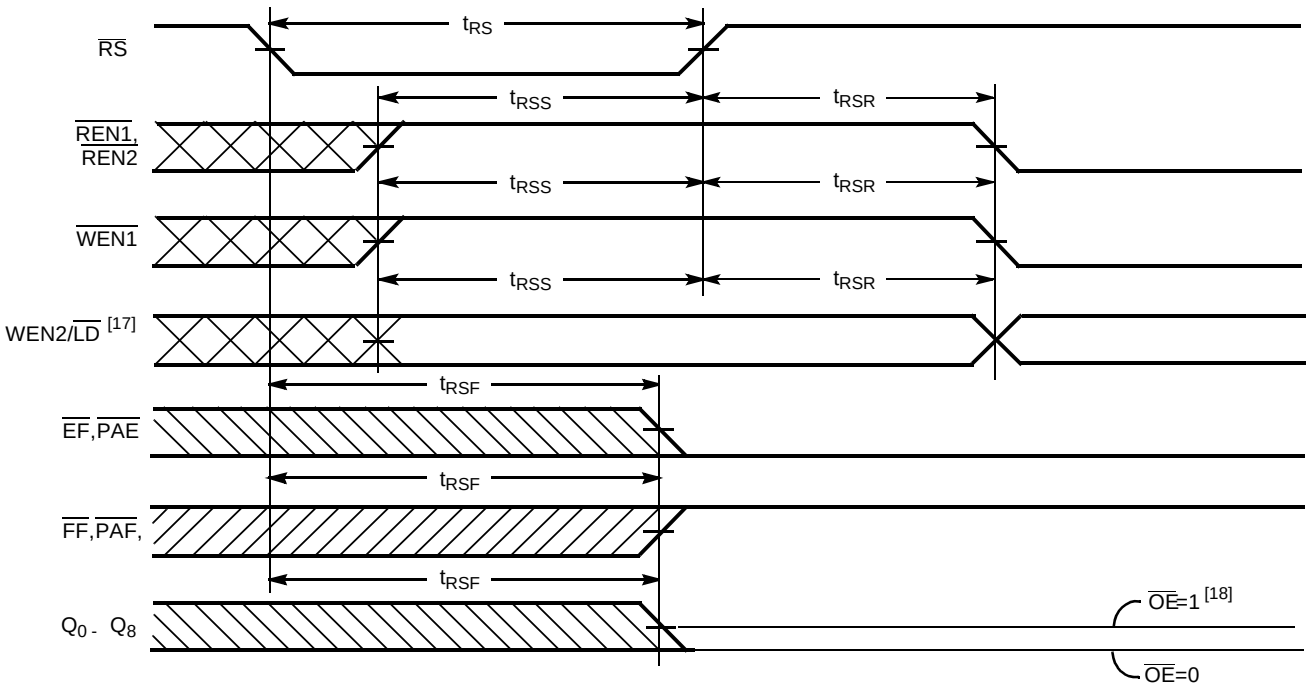
Notes:
12. Pulse widths less than minimum values are not allowed.
13. Values guaranteed by design, not currently tested.

Switching Waveforms (continued)

Read Cycle Timing



Reset Timing[16]

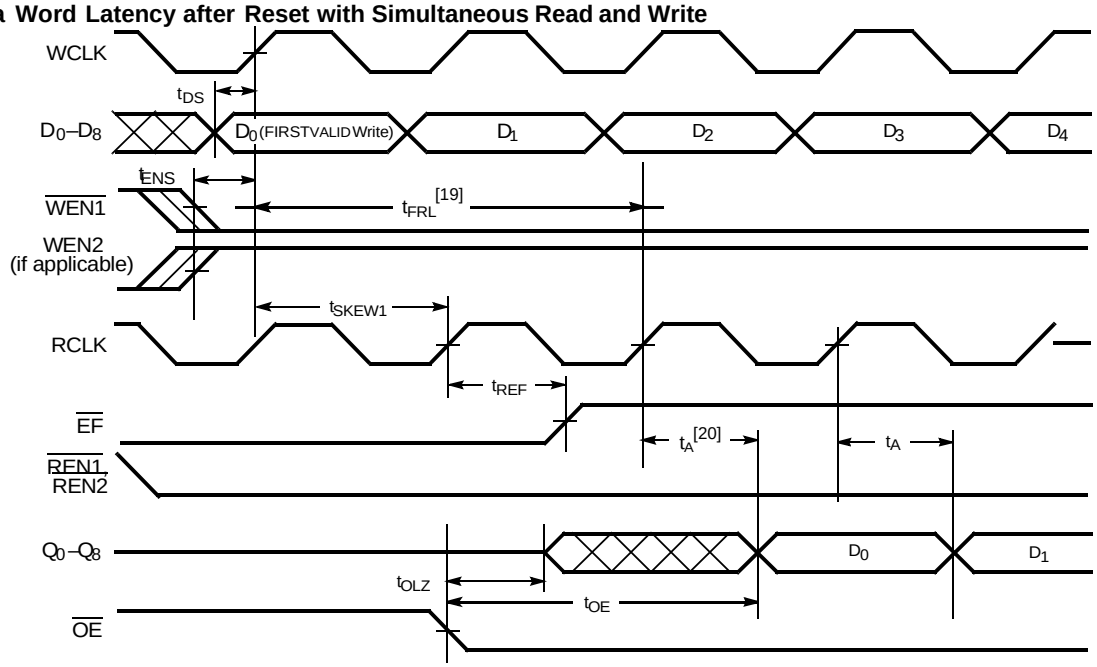


Notes:

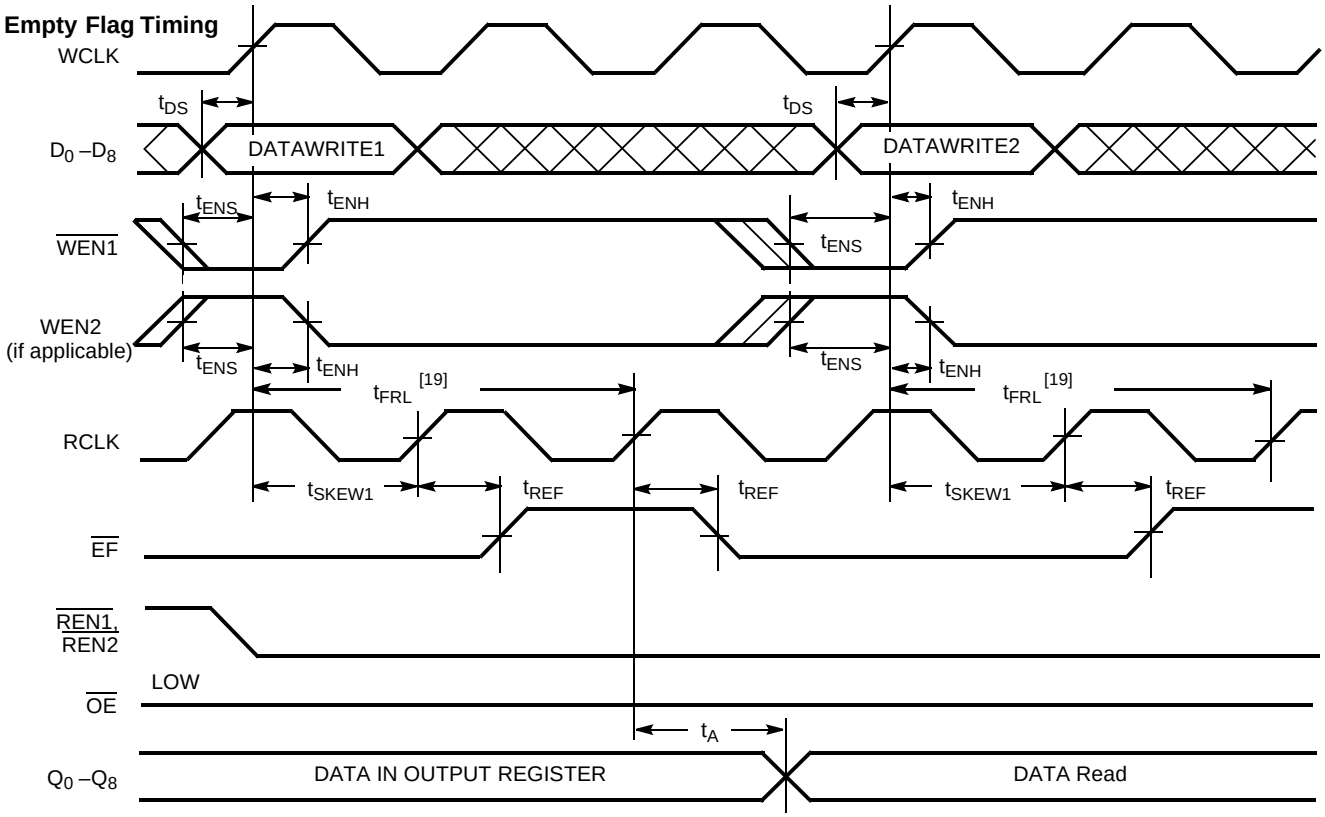
14. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then FF may not change state until the next WCLK rising edge.
15. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

First Data Word Latency after Reset with Simultaneous Read and Write



Empty Flag Timing

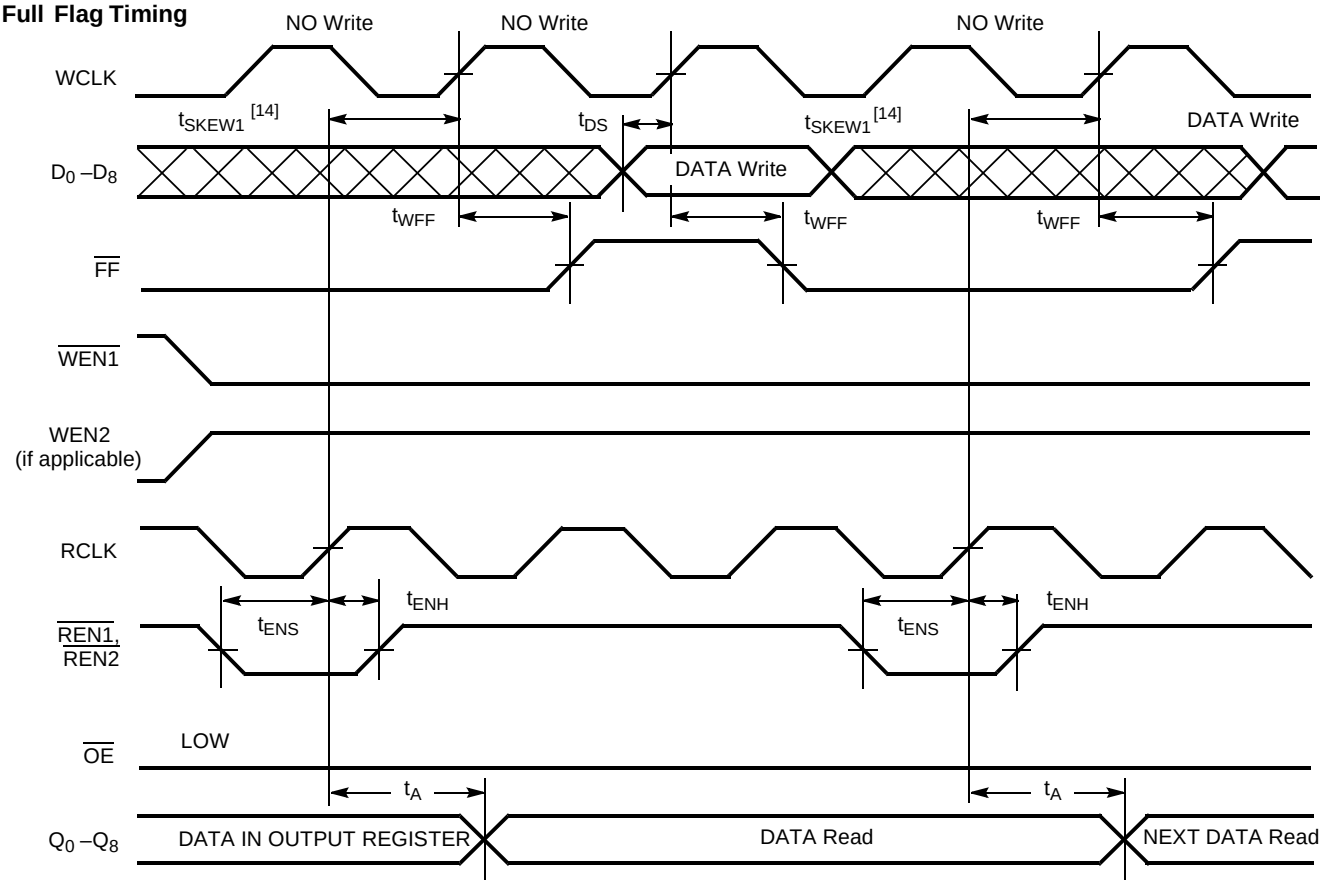


Notes:

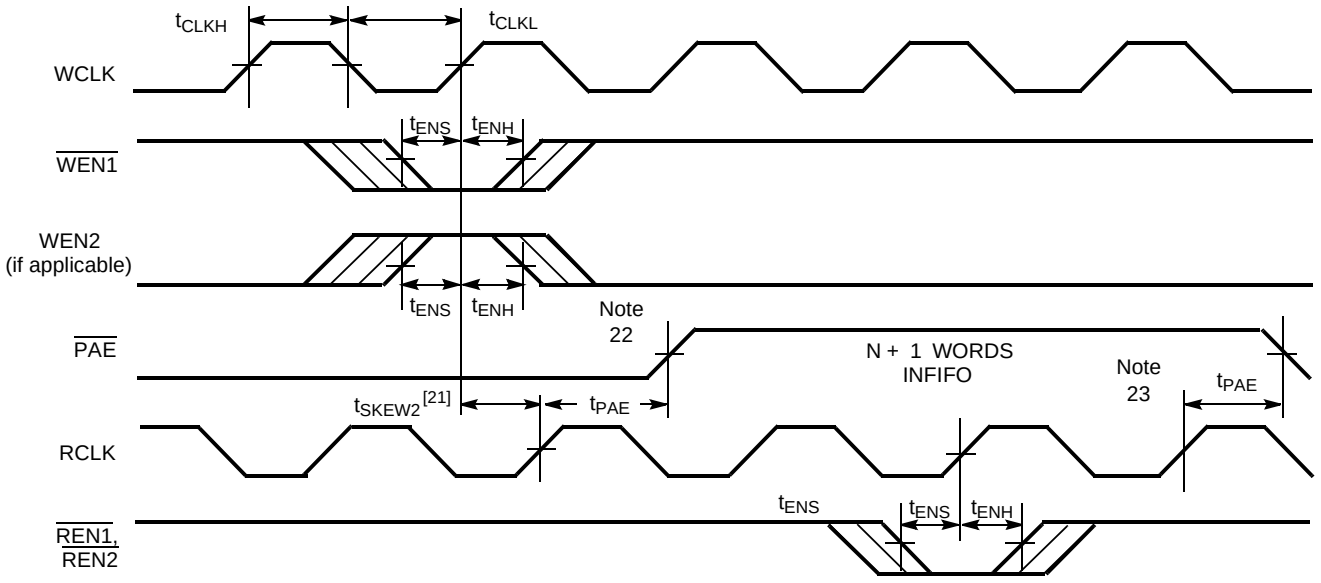
16. The clocks (RCLK, WCLK) can be free-running during reset.
17. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a second enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
18. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$=1.
19. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW1}. When t_{SKEW1} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW1} or t_{CLK} + t_{SKEW1}. The Latency Timing applies only at the Empty Boundary (EF = LOW).
20. The first word is available the cycle after EF goes HIGH, always.

Switching Waveforms (continued)

Full Flag Timing

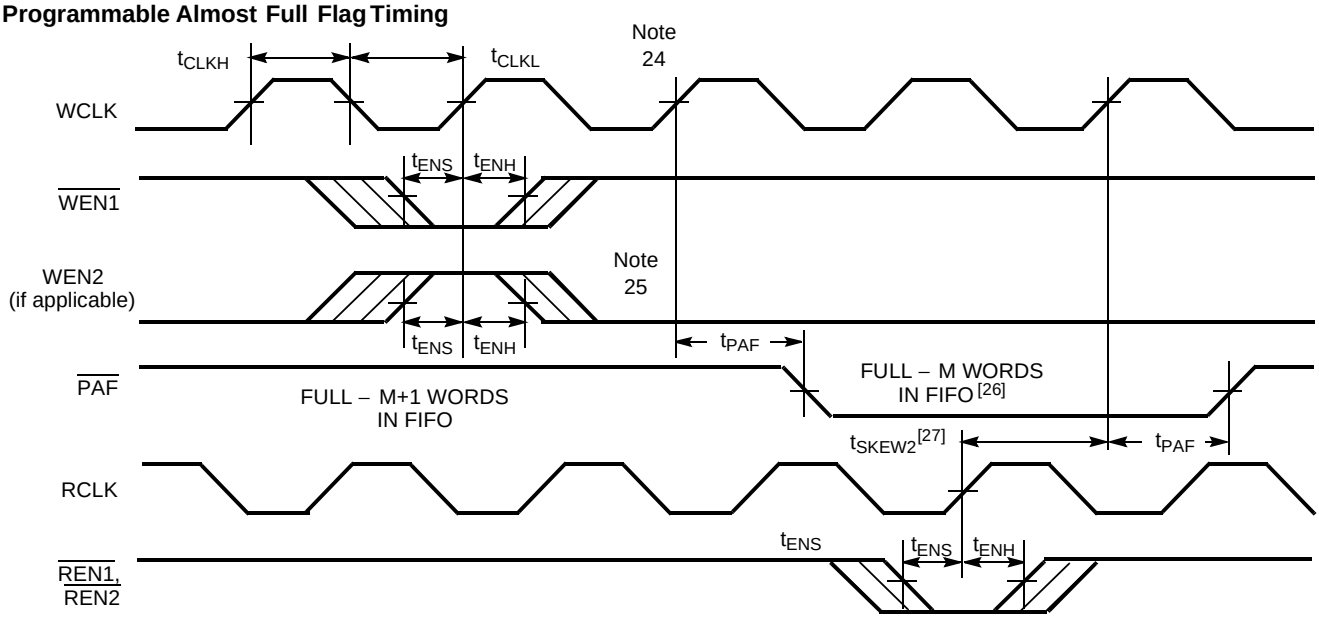


Programmable Almost Empty Flag Timing

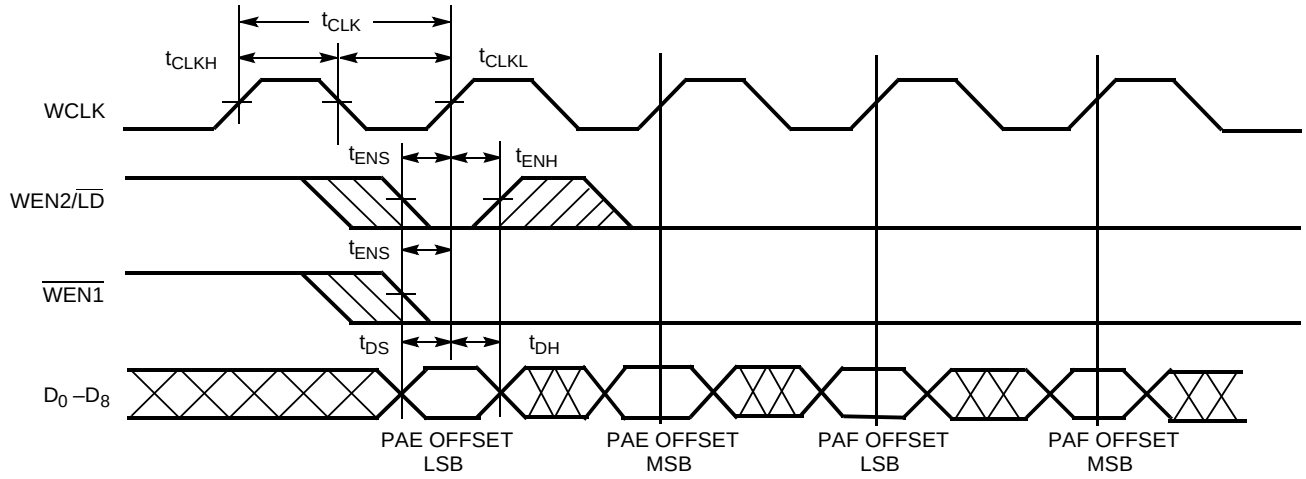


Switching Waveforms (continued)

Programmable Almost Full Flag Timing



Write Programmable Registers

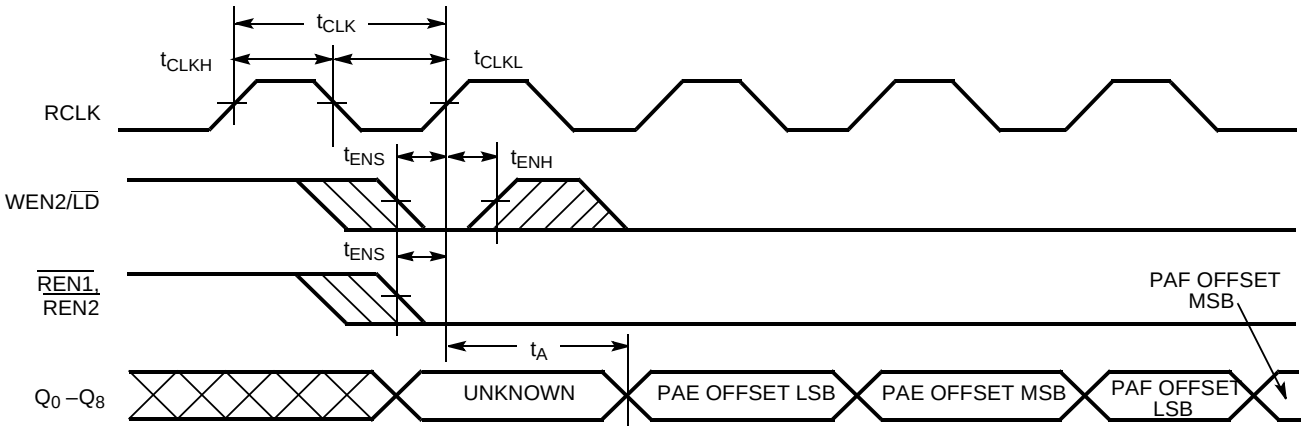


Notes:

21. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then PAE may not change state until the next RCLK.
22. PAE offset = n.
23. If a Read is performed on this rising edge of the Read clock, there will be Empty + (n – 1) words in the FIFO when $\overline{PAE}$ goes LOW.
24. If a Write is performed on this rising edge of the Write clock, there will be Full – (m – 1) words of the FIFO when PAF goes LOW.
25. PAF offset = m.
26. 64-m words for CY7C4421, 256 – m words in FIFO for CY7C4201, 512 – m words for CY7C4211, 1024 – m words for CY7C4221, 2048 – m words for CY7C4231, 4096 – m words for CY7C4241, 8192 – m words for CY7C4251.
27. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

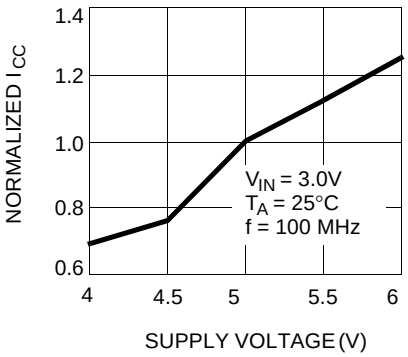
Switching Waveforms (continued)

Read Programmable Registers

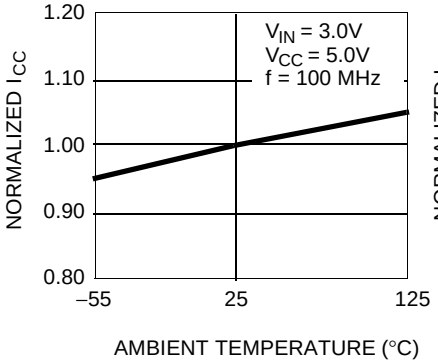


Typical AC and DC Characteristics

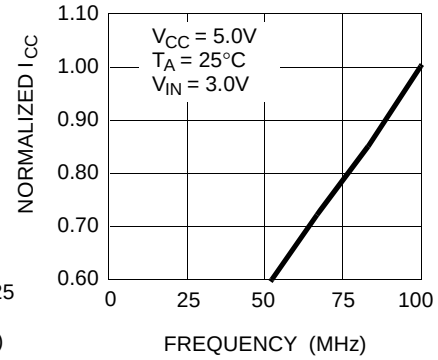
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



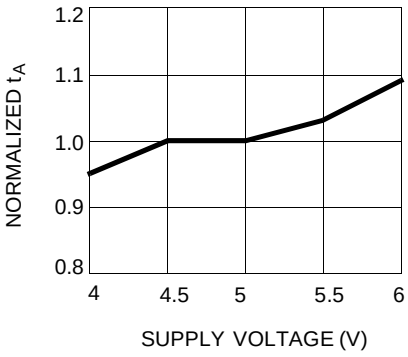
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



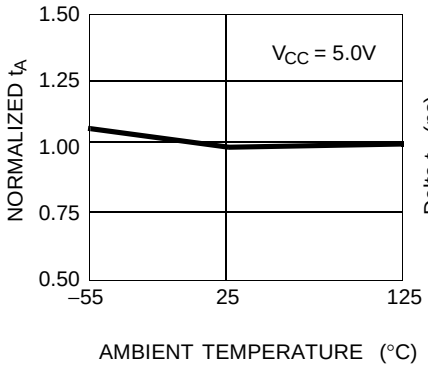
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



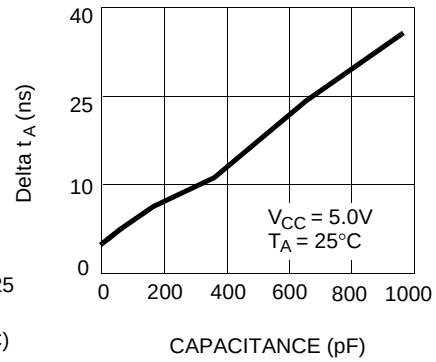
NORMALIZED t_A vs. SUPPLY VOLTAGE



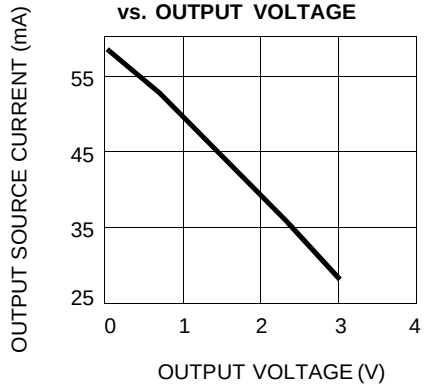
NORMALIZED t_A vs. AMBIENT TEMPERATURE



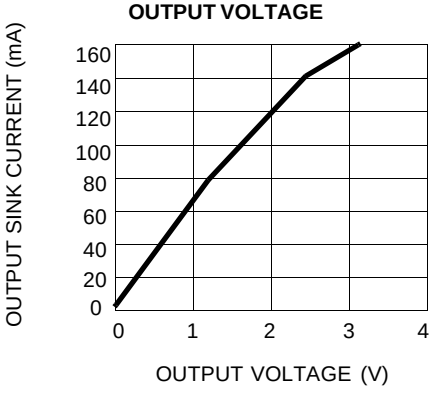
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

64 x 9 Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4421-10AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4421-10JC	J65	32-lead Plastic Leaded Chip Carrier	
15	CY7C4421-15AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4421-15JC	J65	32-lead Plastic Leaded Chip Carrier	

256 x 9 Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4201-10AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4201-10JC	J65	32-lead Plastic Leaded Chip Carrier	
15	CY7C4201-15AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4201-15JC	J65	32-lead Plastic Leaded Chip Carrier	
25	CY7C4201-25AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4201-25JC	J65	32-lead Plastic Leaded Chip Carrier	
	CY7C4201-25AI	A32	32-lead Thin Quad Flatpack	Industrial

512 x 9 Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4211-10AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4211-10JC	J65	32-lead Plastic Leaded Chip Carrier	
	CY7C4211-10AI	A32	32-lead Thin Quad Flatpack	Industrial
	CY7C4211-10JI	J65	32-lead Plastic Leaded Chip Carrier	
15	CY7C4211-15AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4211-15JC	J65	32-lead Plastic Leaded Chip Carrier	
	CY7C4211-15AI	A32	32-lead Thin Quad Flatpack	Industrial
25	CY7C4211-25AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4211-25JC	J65	32-lead Plastic Leaded Chip Carrier	

1K x 9 Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4221-10AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4221-10JC	J65	32-lead Plastic Leaded Chip Carrier	
15	CY7C4221-15AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4221-15JC	J65	32-lead Plastic Leaded Chip Carrier	
25	CY7C4221-25AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4221-25JC	J65	32-lead Plastic Leaded Chip Carrier	

2K x 9 Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4231-10AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4231-10JC	J65	32-lead Plastic Leaded Chip Carrier	
15	CY7C4231-15AC	A32	32-lead Thin Quad Flatpack	Commercial

2K x 9 Synchronous FIFO (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
	CY7C4231-15JC	J65	32-lead Plastic Leaded Chip Carrier	
25	CY7C4231-25AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4231-25JC	J65	32-lead Plastic Leaded Chip Carrier	

4K x 9 Synchronous FIFO

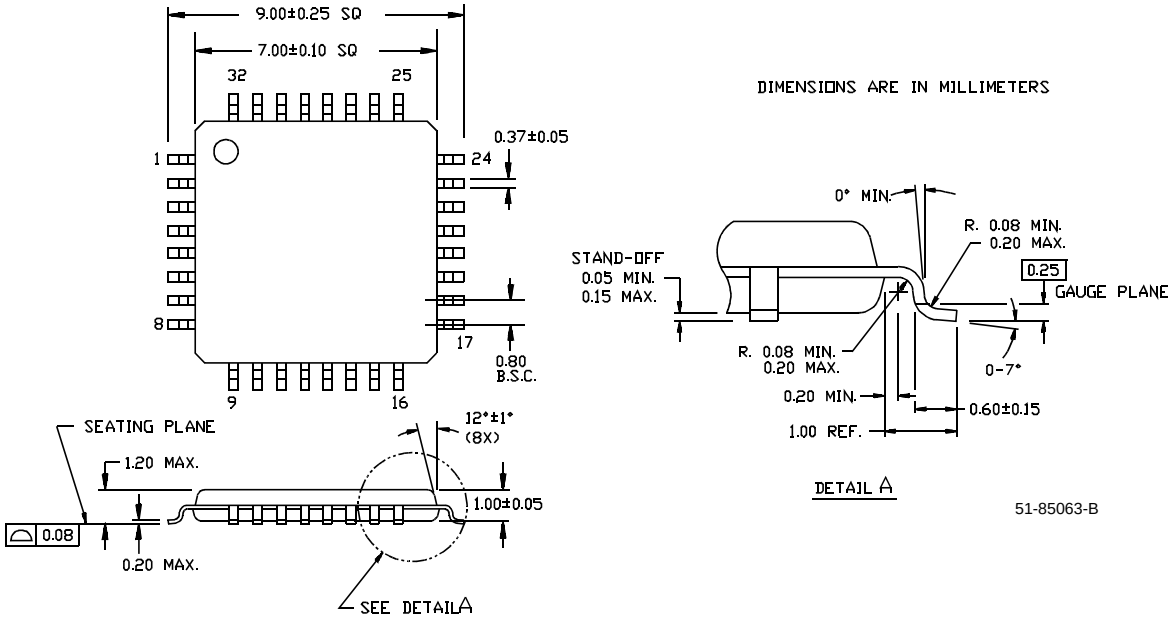
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4241-10AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4241-10JC	J65	32-lead Plastic Leaded Chip Carrier	
	CY7C4241-10JI	J65	32-lead Plastic Leaded Chip Carrier	Industrial
15	CY7C4241-15AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4241-15JC	J65	32-lead Plastic Leaded Chip Carrier	
25	CY7C4241-25AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4241-25JC	J65	32-lead Plastic Leaded Chip Carrier	
	CY7C4241-25JI	J65	32-lead Plastic Leaded Chip Carrier	Industrial

8K x 9 Synchronous FIFO

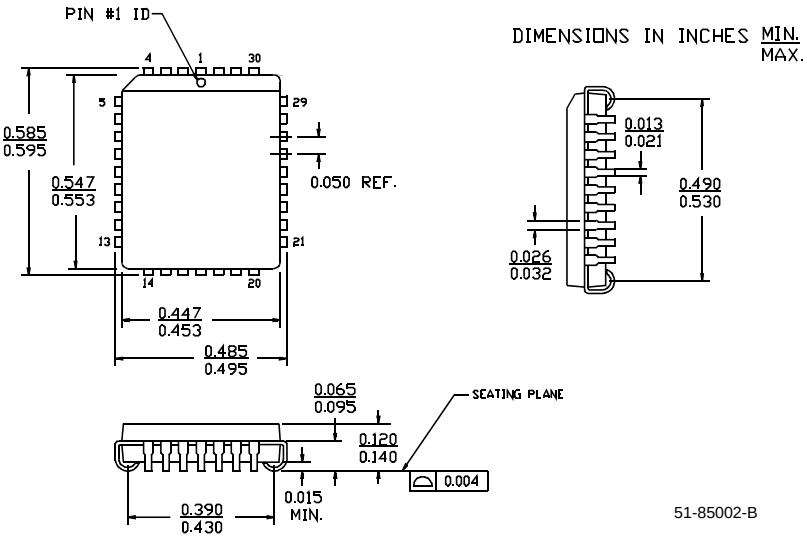
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4251-10AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4251-10JC	J65	32-lead Plastic Leaded Chip Carrier	
	CY7C4251-10AI	A32	32-lead Thin Quad Flatpack	Industrial
15	CY7C4251-15AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4251-15JC	J65	32-lead Plastic Leaded Chip Carrier	
25	CY7C4251-25AC	A32	32-lead Thin Quad Flatpack	Commercial
	CY7C4251-25JC	J65	32-lead Plastic Leaded Chip Carrier	
	CY7C4251-25AI	A32	32-lead Thin Quad Flatpack	Industrial

Package Diagrams

32-lead Thin Plastic Quad Flatpack 7 × 7 × 1.0 mm A32



32-Lead Plastic Leaded Chip Carrier J65



Document Title: CY7C4421/4201/4211/4221, CY7C4231/4241/4251 64/256/512/1K/2K/4K/8K x 9 Synchronous FIFOs Document Number: 38-06016				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106477	09/10/01	SZV	Change from Spec number: 38-00419 to 38-06016
*A	110725	03/20/02	FSG	Change Input Leakage current I_{IX} unit from mA to μA (typo)