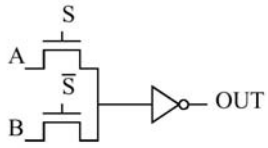
Homework #3

- All Spice problems in this homework are to be done for technologies
  - tsmc_0_35.model (if the last digit of your SSN is odd)
  - tsmc_0_18.model (if the last digit of your SSN is even)
  - Vdd = 3.3 V, default temp
  - all input waveforms should have rise/fall times of 100 ps.

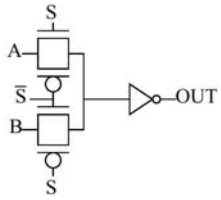
Part A: Compare the following Mux solutions:

1. Y = A S + B S' implemented as a static gate. (2/1 sizing)

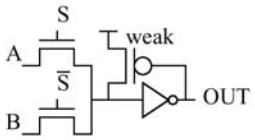
2.



3.

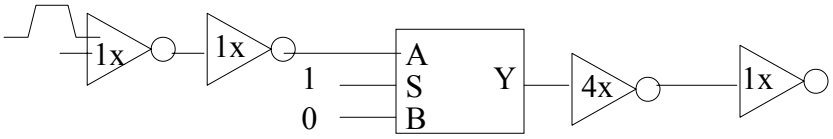


4.



Use 2/1 sizing on output inverter. Use minimum sizing for pass transistors. You choose the sizing for weak pullup and use a split keeper approach.

Test Setup (Part A).

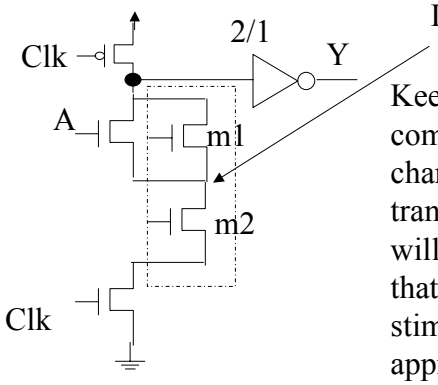


1. Measure average delay (A2Y TPLH + A2Y TPHL)/2

2. Measure power dissipation of mux and 1X inverter driving the mux.. For 0.35u, use a clk input waveform of 500 Mhz. For 0.18 us, use a clock input waveform of 1 Ghz. Give me absolute power dissipation at these frequencies and also as a capacitance value. Use the same power supply for the mux (DUT) and 1X inverter driving the mux, use a different power supply for the other gates.

Part B: Charge Sharing

Answer the following question: When does charge sharing in a domino logic gate become a problem in your technology? (0.35u or 0.18 u)?

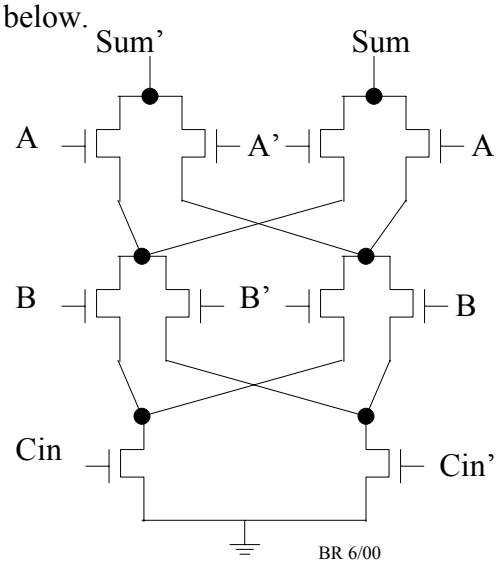


Internal Node capacitance

Keep adding parallel combinations like m1/m2 until charge sharing causes a transition on the Y output. You will need to provide simulations that demonstrate this, and stimulate Node 'A' appropriately. For simplicity, use GEO = 0 for all transistors.

Part C: DVCSL

Use the K-map method to derive the full adder sum logic shown below.



Report

- Present all measurement results in tabular formats in a professional manner
- For Part B, carefully explain how your simulations expose the worst case charge sharing
  - Include output waveforms that demonstrate the charge sharing as well as measurements
- For Part C, simply show your work.
- Comment on all results obtained in Parts A, B.