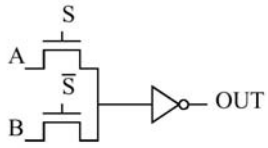
Homework #3

- All Spice problems in this homework are to be done for technologies
  - tsmc_0_35.model (if the last digit of your SSN is odd)
  - tsmc_0_18.model (if the last digit of your SSN is even)
  - Vdd = 3.3 V, default temp
  - all input waveforms should have rise/fall times of 100 ps.

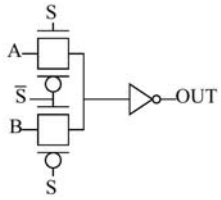
Part A: Compare the following Mux solutions:

1. Y = A S + B S' implemented as a static gate. (2/1 sizing)

2.



3.



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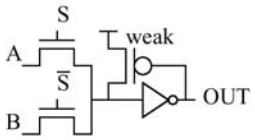
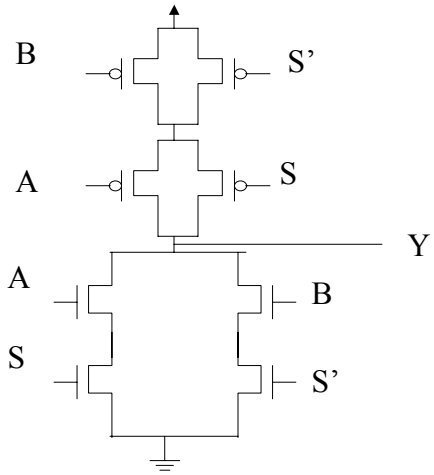


Use 2/1 sizing on output inverter. Use minimum sizing for pass transistors. You choose the sizing for weak pullup and use a split keeper approach.

Static Gate

Note that muxes in parts 2,3,4 actually implement
Y = (A S + B S')' -- this is what I implemented

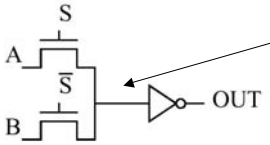


P widths = 4 * Lmin

N widths = 2 * Lmin

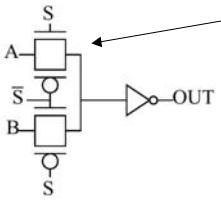
Issues with other mux implementations

2.



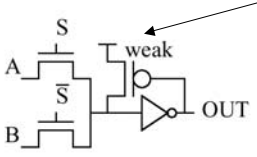
Node at Vdd-Vth if a high value – extra static power dissipation?

3.



Full transmission gates, but more node capacitance – more dynamic power dissipation?

4.



No TGs, fixes Vdd-Vth problem, but slower because has to be overdriven?

0.18u Results (Vdd = 3.3v)

	delay (ps)	power (uW)	cap (fF)
static	46	89	16
pass tran	56	109	62
tran gate	59	80	15
pass tran + pullup	71	91	17

Clk per. = 2 ns (500 Mhz)

	delay (ps)	power (uW)	cap (fF)
static	46	8.9	16
pass tran	56	34	20
tran gate	59	8.0	15
pass tran + pullup	71	9.1	17

Clk per. = 20 ns (50 Mhz)

0.18 u Comments

- Pass transistor + pullup was slowest case
- Static power dissipation was definitely a problem in the pass transistor only case
  - P(avg) in spice measures total power = dynamic + static
  - lowering clock frequency will reduce dynamic dissipation, static power independent of clock frequency
  - difference in power consumption extreme at lower clock frequency
  - static power dissipation not a problem in other muxes
- Static mux compares well

0.35u Results

	delay (ps)	power (uW)	cap (fF)
static	109	116	21
pass tran	152	109	20
tran gate	181	123	23
pass tran + pullup	183	122	22

Clk per. = 2 ns (500 Mhz)

	delay (ps)	power (uW)	cap (fF)
static	109	11.6	21
pass tran	152	13.0	24
tran gate	181	12.4	23
pass tran + pullup	183	12.4	23

Clk per. = 20 ns (50 Mhz)

0.35u Comments

- Static power dissipation in pass transistor mux not nearly as bad at 0.35u as at 0.18u
  - transistors are less leaky
  - static power dissipation pass transistor mux still noticeable at lower clock frequencies
  - pass transistor mux could be viable at .35u
- Transmission gate mux consumes more dynamic power and is slower than pass transistor mux
  - more source/drain capacitance with TGs
- Static looks best

0.18u Results (Vdd = 1.8v)

	delay (ps)	power (uW)	cap (fF)
static	72	25	15
pass tran	108	26	16
tran gate	99	23	14
pass tran + pullup	132	25	16

Clk per. = 2 ns (500 Mhz)

	delay (ps)	power (uW)	cap (fF)
static	72	2.5	16
pass tran	108	5.6	20
tran gate	99	2.3	15
pass tran + pullup	132	2.5	17

Clk per. = 20 ns (50 Mhz)

Comments on 0.18u 3.3v vs. 1.8v

- 3.3v is actually too high for a 0.18u process
- 1.8v to 2.2v is a more reasonable value
- Note that static power dissipation is still a problem with the pass transistor mux
  - at lower frequencies, the pass transistor mux consumes twice the power of the other muxes, principally due to static power consumpation due to the internal node being at Vdd-Vt.
- The static mux is still the overall winner

Misc Issues: Pass transistor sizing

In TG mux, should PMOS pass transistor be 1/1 or 2/1?
Only reason to increase size would be to decrease delay?
Power dissipation will obviously go up.

For 0.35 u: 1/1 sizing, delay = 181 ps
2/1 sizing, delay = 190 ps

For 0.18u: 1/1 sizing, delay = 59 ps
2/1 sizing, delay = 62 ps

This should not surprise you – if a pass transistor is driving a small load, it should be minimum sized.

Misc Issues: Weak pullup sizing

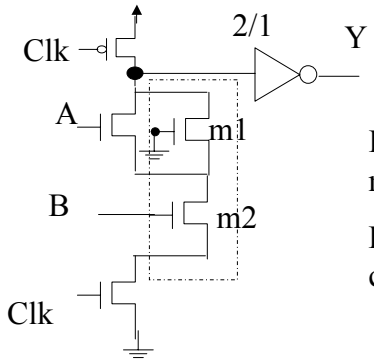
If too strong, gate is slow, and will also increase crowbar power dissipation because fighting strong pullup will keep path between Vdd/GND open longer.

If too weak, then will not stop static power dissipation. Also, making it very weak will mean a long channel, more area (area not a big issue usually, but still needs consideration).

I used split transistor: L = 3 * Lmin for grounded gate device.

For 0.18 u: L = 1 * Lmin: 85 ps, 97 uW (clk per = 2ns)
L = 3 * Lmin: 71 ps, 91 uW (clk_per = 2ns)
L = 5 * Lmin 71 ps, 91 uW (clk_per = 2ns)

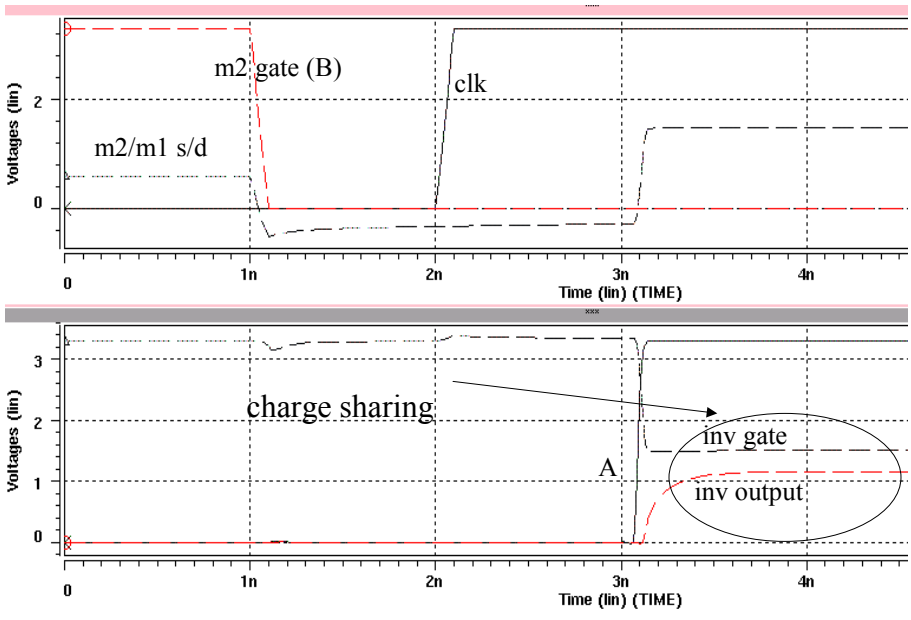
Part B: Charge Sharing



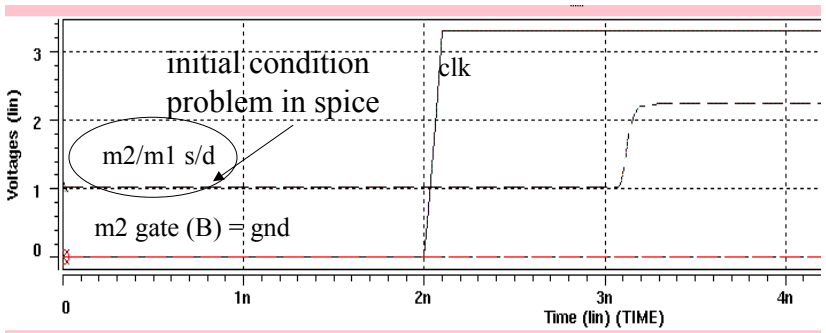
Increased width of both m1, m2.

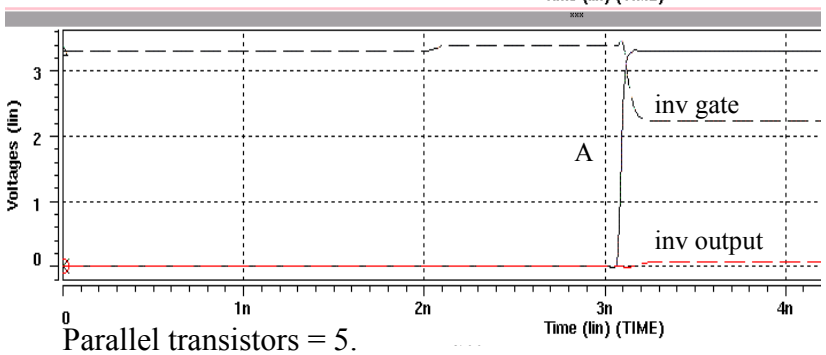
B used to control initial conditions m1/m2 s/d.

When is charge sharing a problem? When Y = Vturnon of next gate = Vtn if driving another domino gate.



Parallel transistors = 5.





Parallel transistors = 5.