FPGA Power Calculations

Summary:	Xilinx (off-line calc,300E) low_route	med_route	Altera (300E)
LUT4	.97 pf	1.5 pf	1.2 pf
DFF	.185 pf (route N/A)		.140 pf

Xilinx included a static power value. This worked out to about 24 uW / CLB, or about 6uW per LUT4.

Spreadsheet results were compatible with Altera Application note figures for the loaded clock tree.

Online Xilinx spreadsheet gave slightly different results from offline version. Answers varied slightly depending upon what devices were used.

Mistakes

- Xilinx CLB slice = 2 LUT4s, needed to account for this
- Do not USE total power figure for Xilinx, this included static power disspation
- Altera included clock tree capacitance as a fixed value for particular die (Same for 200E, 300E; increased for 600E, 1000E because of larger die)
  - When Clock Frequency = nonzero, resulted in non-zero power. If you set toggle freqency to zero, this power did not change as the CLBs were changed, only changed with frequency. This meant it was the clock tree power.
  - Had to SUBTRACT this power number from the LE power number before calculating LE Capacitance, else got too high a value of LE capacitance.
  - Clock tree cap = 510 pf for 200E,300E; 825 pf for 600E,1000E.
  - Xilinx 'cheated' by distributing its clock tree cap (a fixed value per die) among the DFFs. That is why Xilinx DFF cap higher than Altera.

Xilinx Procedure for DFF Cap. (off-line calculator)

- Set the clock freq to some value (say 100 Mhz).
- Set DFFs to some large value (say 1000).
- Offline calculator made you input a CLB value that was at least ½ the number of DFFs since 1 CLB slice has 2 DFFs.
  - You needed to make sure that these CLBs did not contribute to the power number by setting toggle rate to 0 %.
  - The toggle rate refers to how often CLBs switch per clock cycle.
  - The toggle rate for DFFs is always 100% since DFFs consume power every clock.
  - Setting toggle rate to 0% means that CLBs will never switch, thus will not consume power, and the power figure will be all due to the DFFs.
- Record power from row in spreadsheet, calculate cap value based on power equation:

Pwr = Cdff * #Ndffs * Freq * Vdd* Vdd.

Xilinx Procedure for LUT4 Cap. (off-line calculator)

- Set CLBs to some large value (say 1000).
- Set DFFs to zero.
- Set toggle rate to some non-zero value. An easy value is 100%

Pwr = Cclbs * #Nclbs * Toggle% * Freq * Vdd* Vdd.

Because 1 CLB slice = 2 LUT4, had to divide calculated capacitance figure by 2.

Altera Procedure LUT4s, DFFs

- The procedure for Altera was the same except that that the spreadsheet power included the clock tree power (varied only with clock frequency).
- You could see this contribution by setting the LEs to some non-zero value (say 1000), Frequency to some value (100 Mhz), and DFFs to zero, and Toggle Rate to 0.
  - In the Xilinx spreadsheet, this would give a 0 power value because toggle value is 0% and there are no DFFs.
  - In the Altera spreadsheet, this gives a power figure.
  - If you change the # of LEs, the power figure remained constant. In fact, you could set the # of LEs to 0! This power figure only varied with clock frequency, so it MUST be the clock tree.
- When calculating the DFF, LE cap values, you had to subtract off this constant power due to the clock tree before computing the capacitance figure.