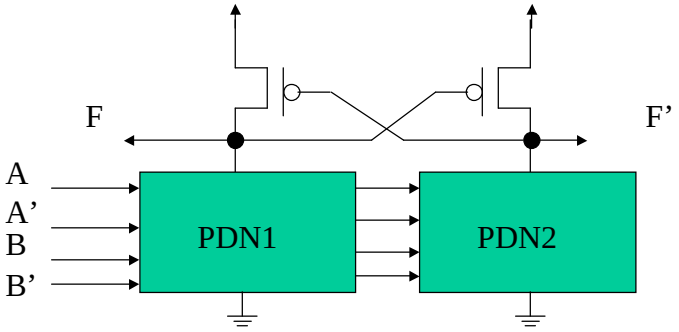
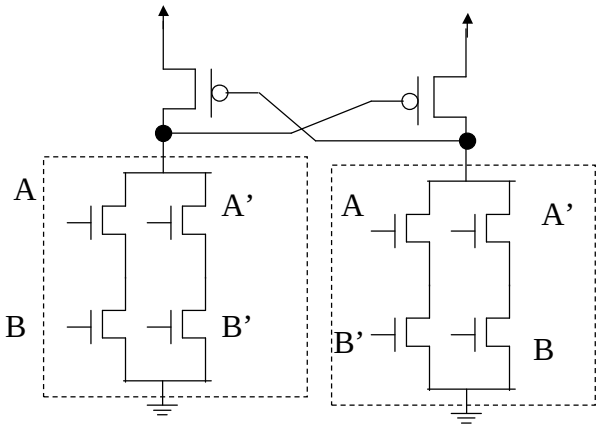
Differential Logic

DCVSL – Differential Cascade Voltage Switch Logic



Both PDN networks are never conducting at same time

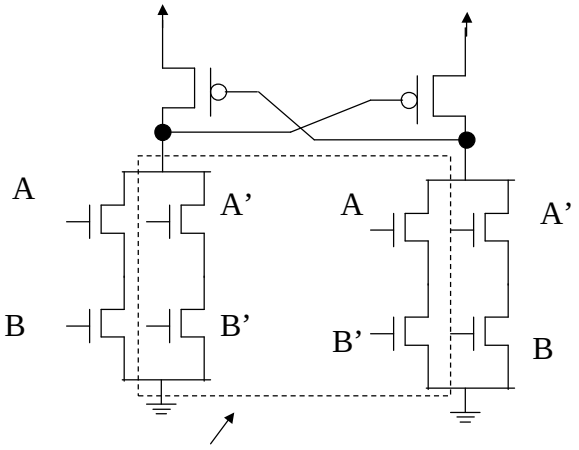
An XOR gate



N1 tree = AB + A'B' N2 tree = A'B + AB'

We can reduce transistor count

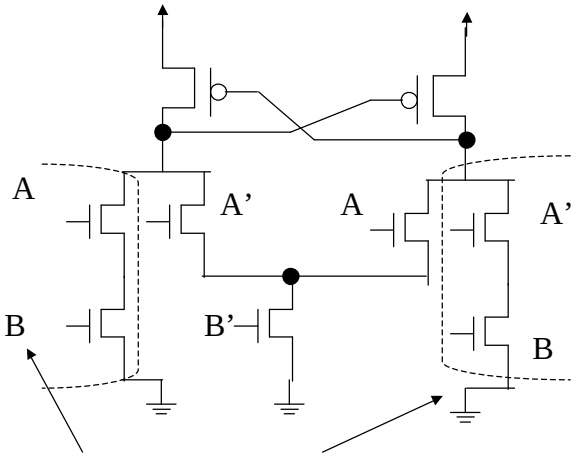
Look for that path is of form X(Y + Y')



Can share the B' transistor

We can reduce transistor count (cont.)

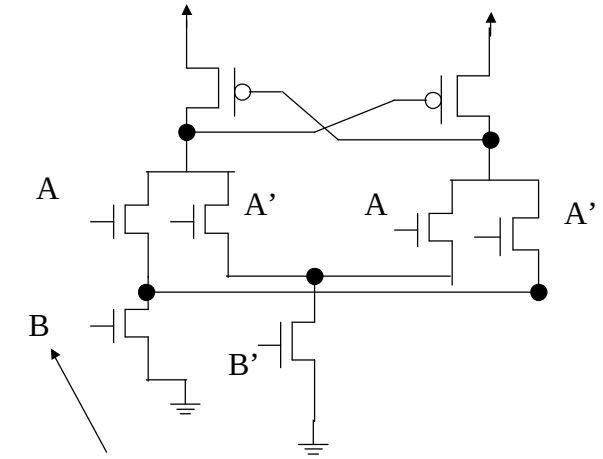
Look for that path is of form X(Y + Y')



Can share the B transistor

We can reduce transistor count (cont.)

Look for that path is of form X(Y + Y')

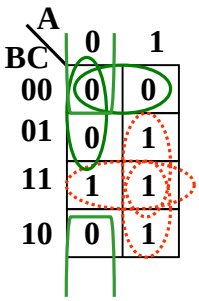


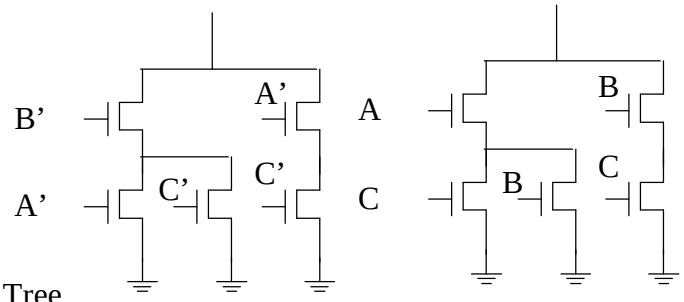
Can share the B transistor

Another Example

Q = ab + bc + ac

10 transistors





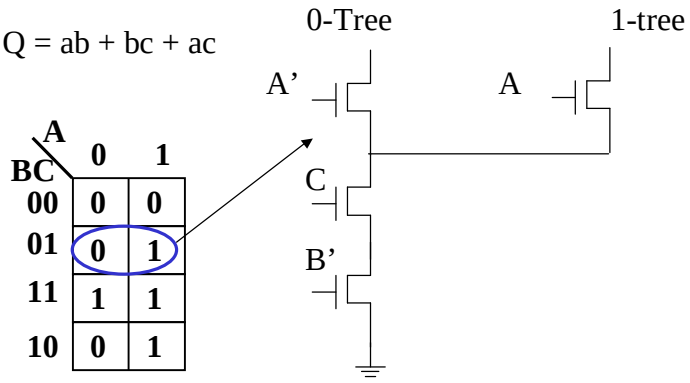
'0' Tree

'1'Tree

We Can Do Better

Remember that to share transistors between ‘0’, ‘1’ trees, we look for X(Y+Y’) structures. Build shared cubes first.

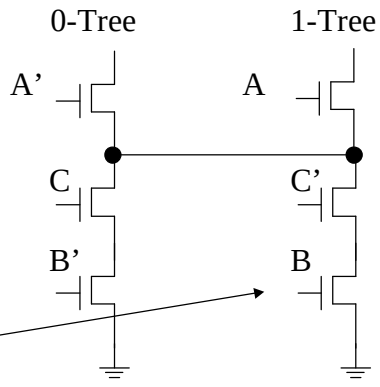
Q = ab + bc + ac



BC \ A	0	1
00	0	0
01	0	1
11	1	1
10	0	1

We Can Do Better (cont.)

Q = ab + bc + ac

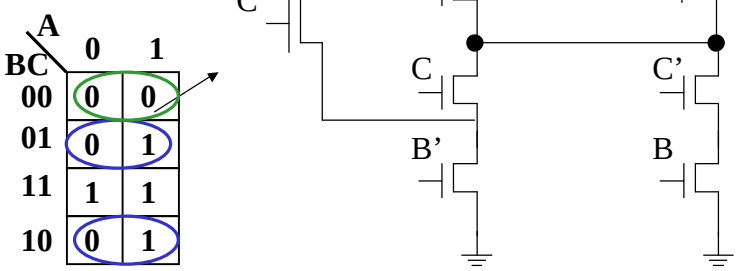


BC \ A	0	1
00	0	0
01	0	1
11	1	1
10	0	1

We Can Do Better (cont.)

Add other cubes to complete.

Q = ab + bc + ac



BC \ A	0	1
00	0	0
01	0	1
11	1	1
10	0	1

We Can Do Better (cont.)

Finished, 8 transistors.

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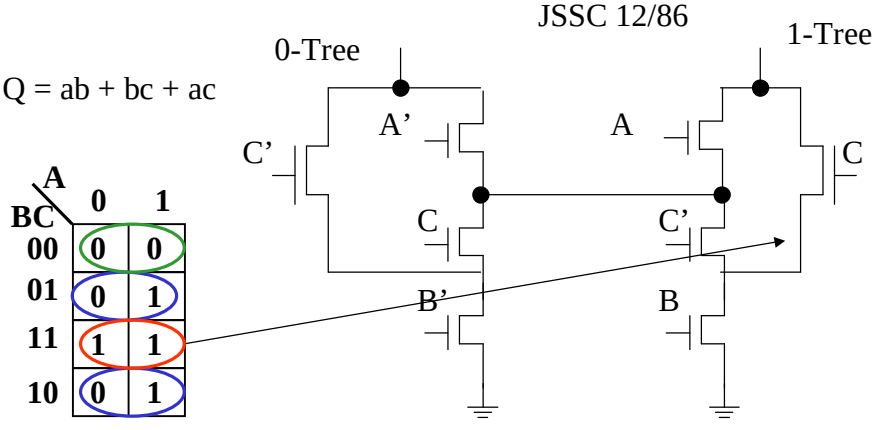
JSSC 12/86

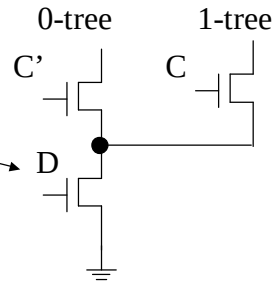
Q = ab + bc + ac



BC \ A	0	1
00	0	0
01	0	1
11	1	1
10	0	1

Another Example

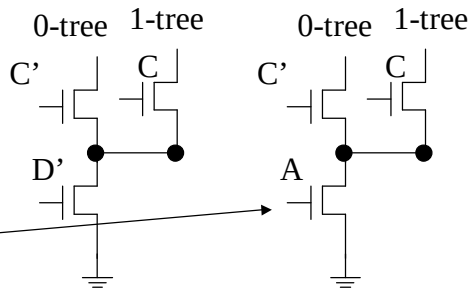
CD \ AB	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	1	1	1



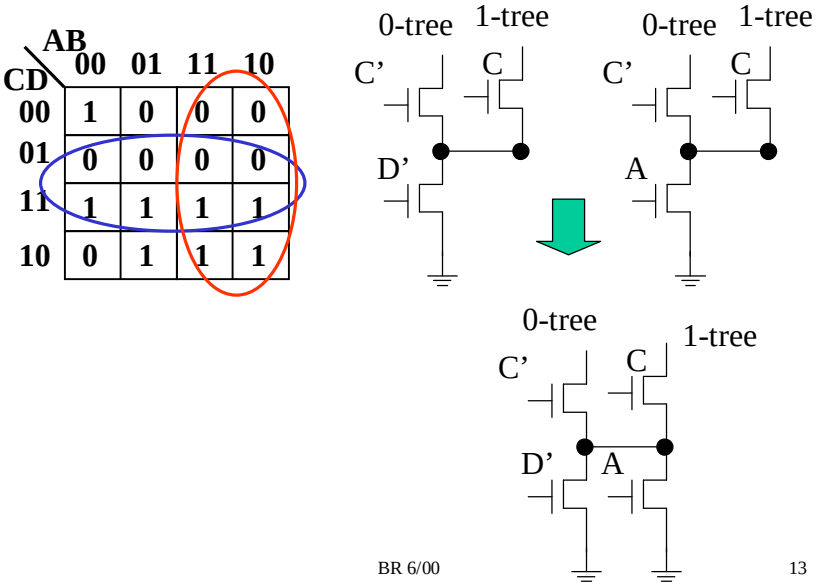
F = A'B'C'D + AC + BC + CD

Another Example (cont.)

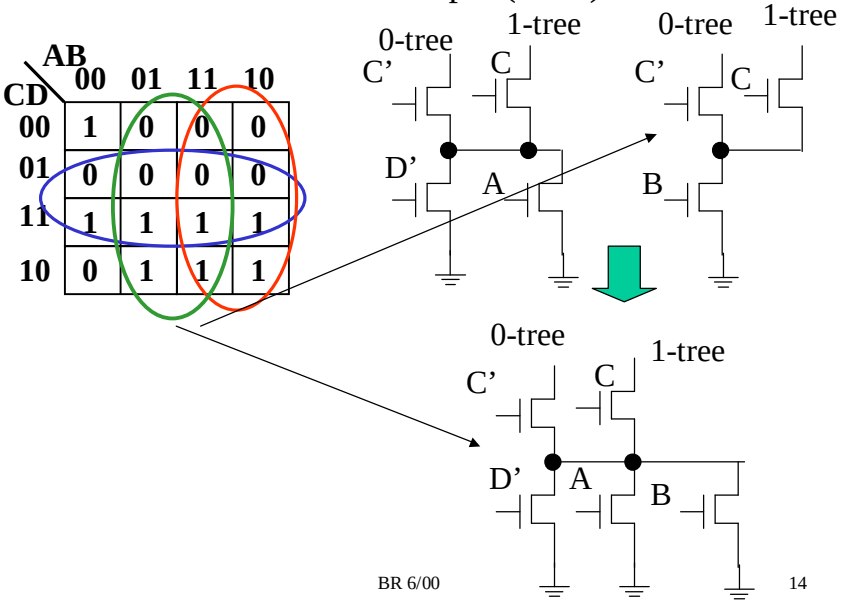
CD \ AB	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	1	1	1



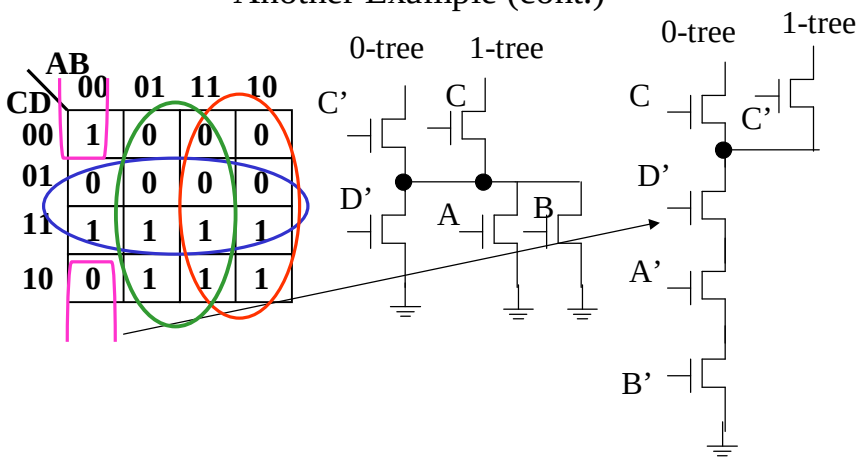
Another Example (cont.)

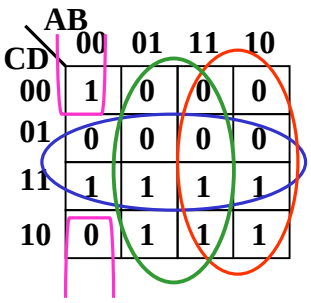


Another Example (cont.)

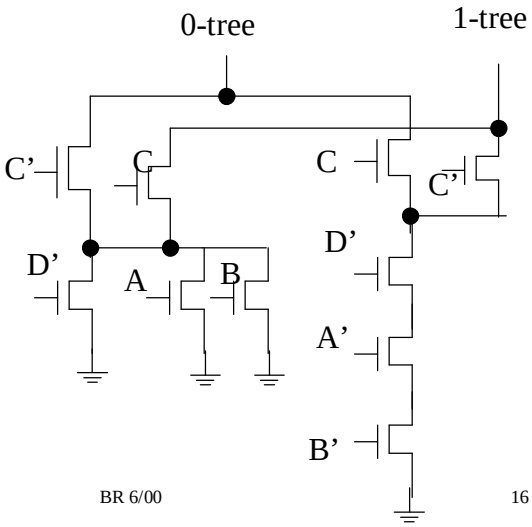


Another Example (cont.)

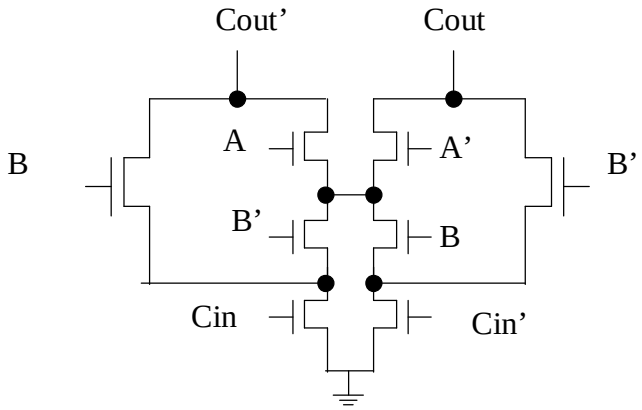




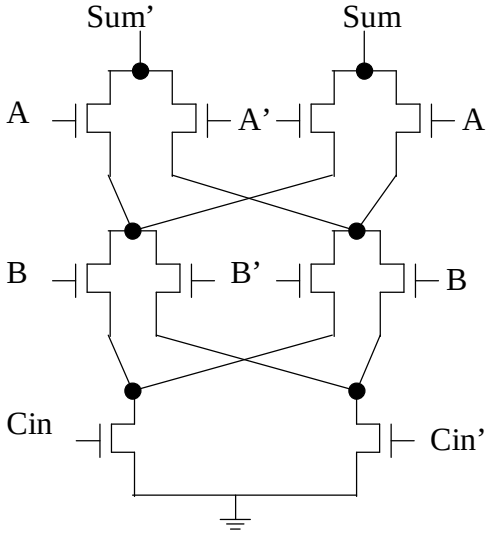
Final Gate, 10 transistors



Full Adder, Cout logic



Full Adder, Sum logic



DCVSL

- Reduces Ptree to a single transistor
- Requires dual rail inputs, increased routing.
- Produces dual rail outputs for other DCVSL gates.
- Produces a good Full Adder implementation, Xor implementation.