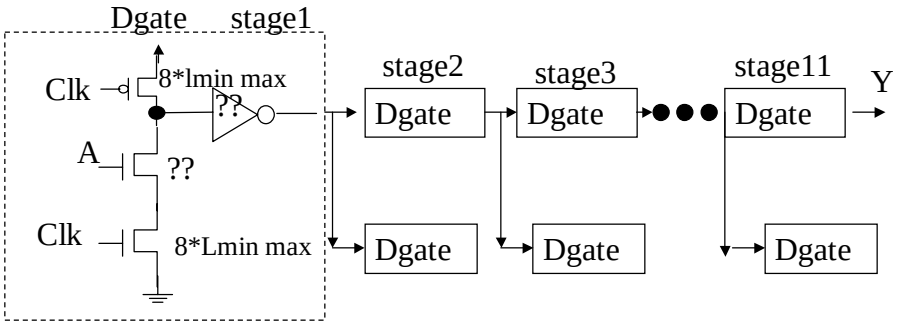
Problem #1: Domino Logic Sizing



For the 11 stage circuit above, size via simulation the output inverter, and the NMOS pulldown of the DGATE such that the A to Y average delay is within 10% of the minimum delay with the lowest dynamic power consumption. You must not exceed the maximum sizes shown on the precharge/eval transistors. Your clock can be any duty cycle you wish. Note that all DGates are the same size. Use 100 ps rise/fall times on both A,Clk signals. Use Leda 0.25u, Vdd = 2.5. (note: Lmin = .25u).

Problem #2

Refer to problem #21, Chapter 4 in the Rabaey textbook. Scale the transistor sizes to the Leda 0.25u , use 2.5 V, and do parts a, b, c of the problem.

Use the GEO parameter on your MOSFETs to indicate source/drain diffusion sharing where applicable. Draw a stick diagram of the layout to support your diffusion sharing assumptions. Assume Gate1, Gate2 are seperate layout blocks.