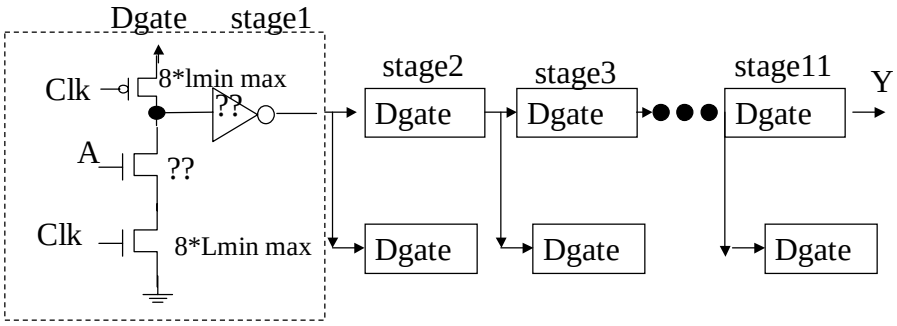
Problem #1: Domino Logic Sizing



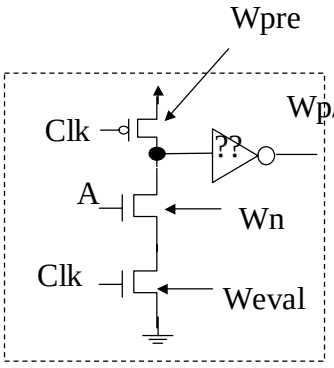
For the 11 stage circuit above, size via simulation the output inverter, and the NMOS pulldown of the DGATE such that the A to Y average delay is within 10% of the minimum delay with the lowest dynamic power consumption. You must not exceed the maximum sizes shown on the precharge/eval transistors. Your clock can be any duty cycle you wish. Note that all DGates are the same size. Use 100 ps rise/fall times on both A,Clk signals. Use Leda 0.25u, Vdd = 2.5. (note: Lmin = .25u).

Solution to #1

A caveat: there are probably multiple solutions that meet the criteria.

First, what to size?

The Wpre and Weval could be given maximum sizes of 8*Lmin.



Wp/Wn*Bufsize = ??

Warning: in all simulations that follow, did not use any GEO parameters. Could have used GEO to indicate source/drain sharing between A, Clk n-transistors.

Try some extremes

pre=8	eval=8			
	Skewed, N=4			
	Eval time	Eval/stg	pre	clk per
Buffsize				
2	1471	134	257	1729
2.5	1438	131	264	1702
3	1418	129	265	1683
3.5	1416	129	267	1683
4	1428	130	265	1693

Large Weval, Wpre, Wn. High Skew output (2/.5 * Buffsize)

pre=1	eval=1			
	Skewed, N=1			
	Eval time	Eval/stg	pre	clk per
Buffsize				
2	1261	115	326	1587
2.5	1328	120	355	1682

Min Weval, Wpre, Wn. High skew output (2/.5 * Buffsize)

Small Sizes worked better.

Start at low end, begin increasing sizes of Eval, Pre, and Wn.

Pre ↑ would Precharge Time ↓, Eval Time ↑

Eval ↑ would Precharge Time ↑, Eval Time ↓

Since eval time decreases are summed over number of stages, better to decrease Eval time at expense of precharge time.

Eventually found good solution to be:

pre=2	eval=8			
	Skewed, N=1			
	Eval time	Eval/stg	pre	clk per
Buffsize				
2	1222	111	294	1516
2.5	1273	116	319	1592

Weval = 8
Wpre = 2,
Wn = 1
High skew output (2/.5 * 2)

Adjust Skew

Was using a buffer sized as Wp/Wn = 4/1 (high skew)

Looked at changing skew in both directions to see if this would improve delay.

Found that Wp/Wn = 3/1 gave minimum delay.

pre=2	eval=8			
	Skew 3/1, N=1			
	Eval time	Eval/stg	pre	clk per
Buffsize				
2	1232	112	273	1504
2.5	1259	115	289	1548

Weval = 8
Wpre = 2,
Wn = 1
Slightly high skew output (3/1)

Reduce power

Min. Delay was approximately 1500 ps.
+10% delay = 1650 ps. Go to minimum size with no-skew output, adjust from there.

			Pwr in uW		Tot. Pwr	%diff
Wpre=2, Weval=8	Clk Per.	%diff	Vdd	Clk		
Wn=1, Buff=3/1	1504		198	14	212	
Wpre=1, Weval=1						
Wn=1, Buff=2/1	1286	3.0%	135	3.6	138.6	-34.6%
Wpre=1, Weval=1						
Wn=1, Buff=1.5/1	1586	5.5%	124	3.5	127.5	-39.9%
Wpre=1, Weval=1						
Wn=1, Buff=1/1	1709	13.6%	113	3.5	116.5	-45.0%

Saved approx 40% in power at cost of 5.5% in delay.

Problem #2

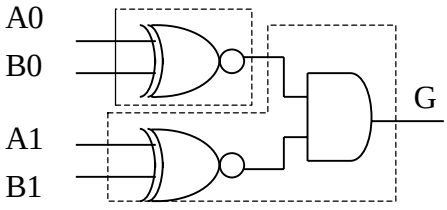
Refer to problem #21, Chapter 4 in the Rabaey textbook. Scale the transistor sizes to the Leda 0.25u , use 2.5 V, and do parts a, b, c of the problem.

Use the GEO parameter on your MOSFETs to indicate source/drain diffusion sharing where applicable. Draw a stick diagram of the layout to support your diffusion sharing assumptions. Assume Gate1, Gate2 are seperate layout blocks.

Circuit Function

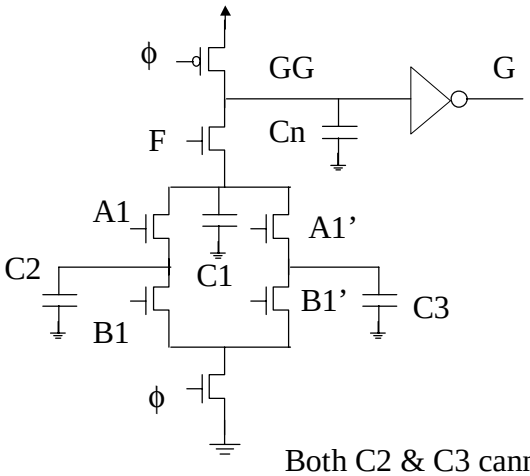
F = A0 B0 or A0' B0' = A0 xnor B0

G = F and (A1 B1 or A1' B1') = F and (A1 xnor B1)



G =1 when A1 A0 = B1 B0, equality circuit

Charge Sharing analysis



Worse case occurs when: C1,C2 or C1,C3 precharged low, Cn precharged high, and during evaluation Cn is supposed to remain high (no path to ground but path to either C2 or C3).

Both C2 & C3 cannot affect Cn because of A1, A1'

Input Sequence

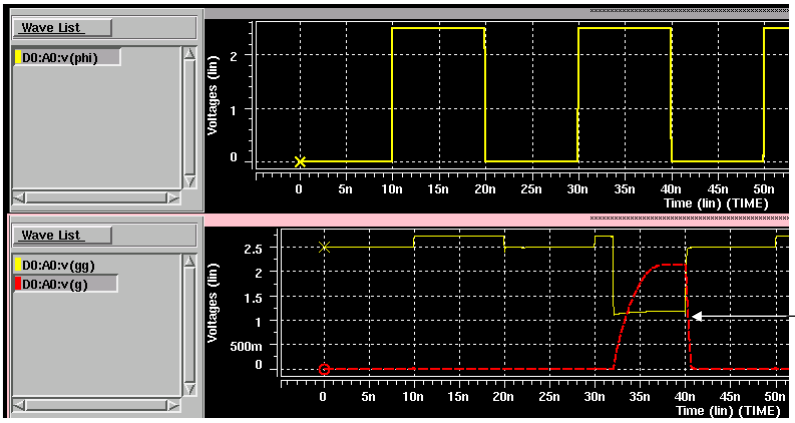
Need C1, C2 precharged low.

First clock, have F=0 (A0=1, B0=0), and A1=1, B1=1. This set C1,C2 = 0.

Second clock, need F=1 (A0=1, B0=1) so we have access to node Cn. Also need access to Node C2 (A1 =1), but C2 needs to be cutoff from ground (B1=0).

Note: if you just test this circuit using all 16 possible combinations of A1,B1,A0, B0 will not necessarily see charge sharing problem. Charge storage makes this a sequential circuit!!! (behavior depends on previous input sequence!!!)

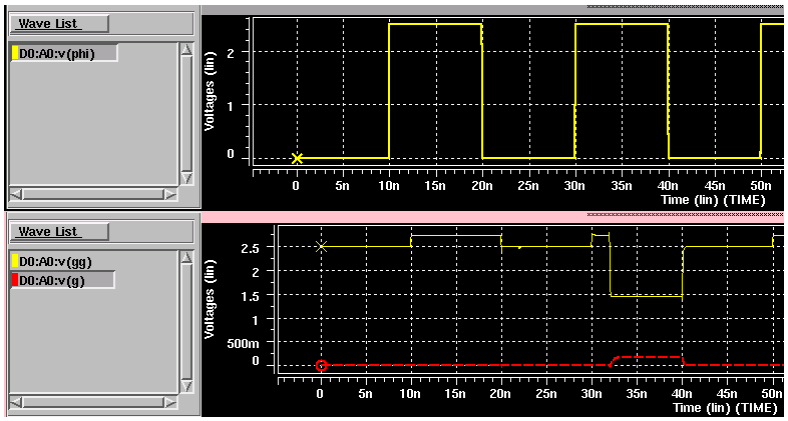
Charge Sharing Problem. Input sequence.
1st clock: A1A0= 11, B1B0: 10, 2nd clock: A1A0:11, B1B0:01
G output should be 0, but is 1. Internal node GG drops.



G

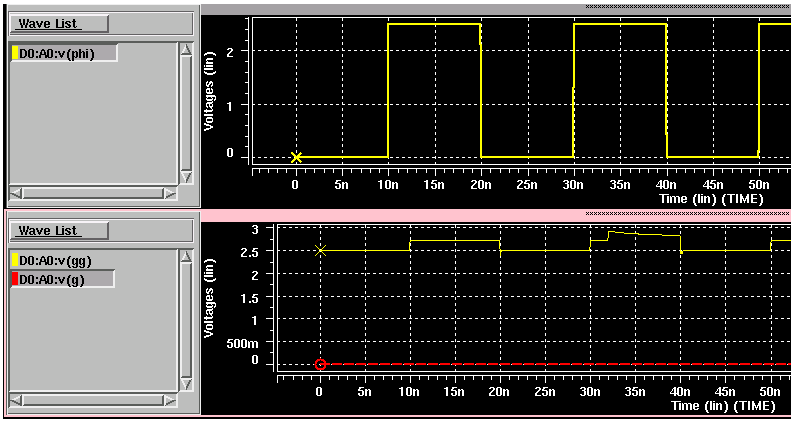
Pre = 4*Lmin width, High Skew inverter 4/1, no GEO parameters.

With GEO params, charge sharing not apparent on output.



Pre = 4*Lmin width, High Skew inverter 4/1, with GEO parameters. GEO parameters with source/drain sharing reduced node capacitance so output only about 0.3 v.

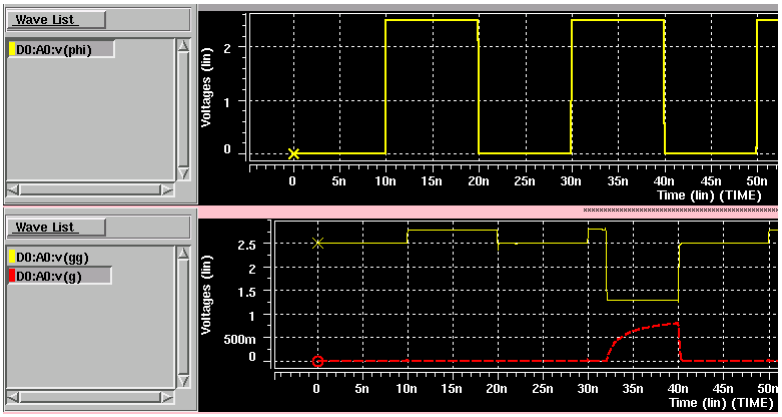
Use extra precharge transistor to eliminate charge sharing.



Pre = 4*Lmin width, High Skew inverter 4/1, no GEO parameters.

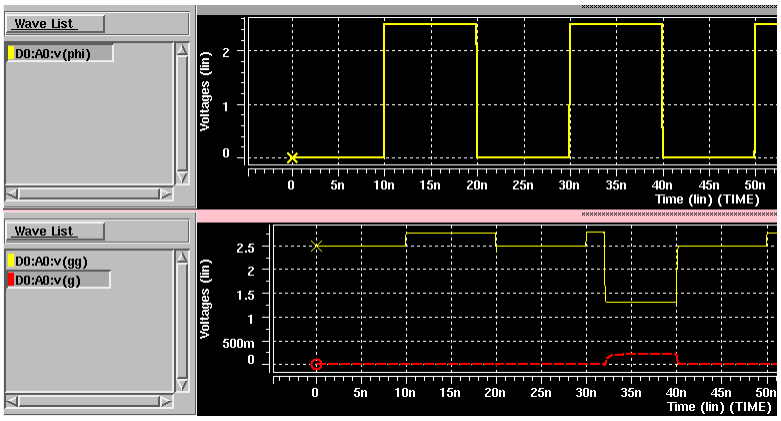
With extra pre-charge transistor to eliminate charge sharing.

Effect of Precharge Width on Charge sharing



No extra precharge transistor, Pre width at 8 * Lmin, high skew output inverter, No GEO. Output high enough to cause concern.

Effect of Inverter skew on output value



No extra precharge transistor, Pre width at 8 * Lmin, normal skew inverter, No GEO. Normal skew inverter has higher threshold, so input not as susceptible to charge sharing.

Delays

	Times in ps
No Geo	Tplh
Inv 4/1, Pre=4*Lmin	461
Inv 4/1 Pre=4*Lmin, extra Pre tran	474
Inv 4/1, Pre=8*Lmin	500
Inv 2/1, Pre=8*Lmin	524
With Geo	
Inv 4/1, Pre=4*Lmin	447

Observations

- Larger precharge transistors adds extra source diffusion capacitance, which offsets charge sharing
- High skew inverter speeds circuit, but lower input threshold makes it more susceptible to threshold sharing.
- Extra precharge transistor slows circuit because more internal node capacitance.
- GEO parameters reduced internal node capacitance so charge sharing not visible on output.