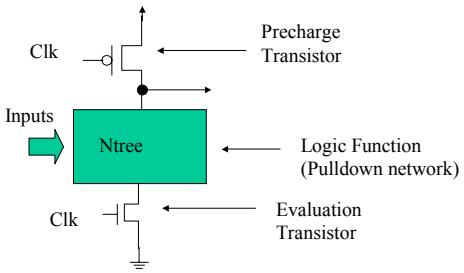
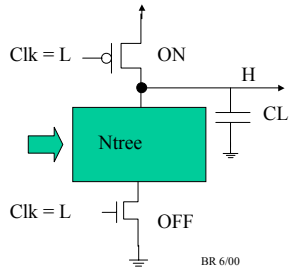
Dynamic Gates



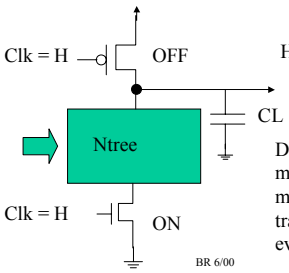
Operation of a Dynamic Gate

- Precharge phase: Clock Low, Precharge transistor on, output pull high. Evaluation transistor off.



Operation of a Dynamic Gate (cont)

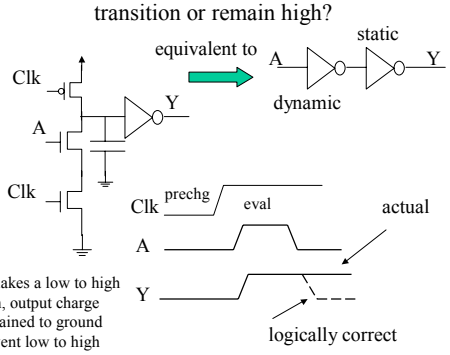
- Evaluation phase: Clock H, Precharge transistor off, Evaluation transistor on. Output is pulled low if a there is a path in Ntree to ground.



H → L or output remains high

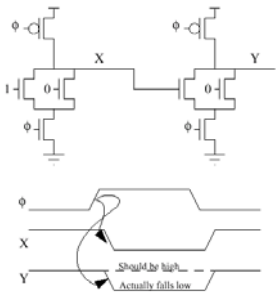
During evaluation, inputs must either remain high or make a single low to high transition within evaluation period

Why must gate input only make a single low to high transition or remain high?



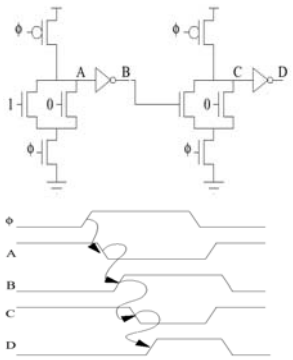
Input A makes a low to high transistion, output charge already drained to ground when A went low to high

Cascading Dynamic Gates



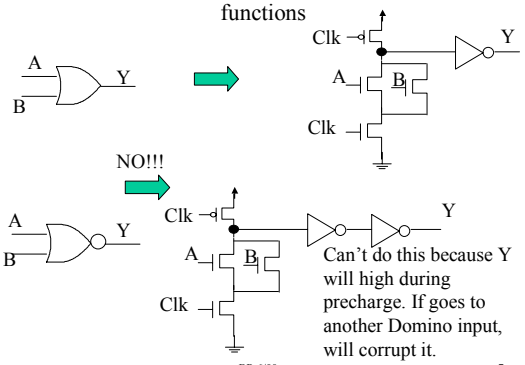
X input to 2nd gate violates transistion rule and makes a high to low transition. Because X was high to begin with, charge on Y node was discharged to ground before X transistioned to 0.

Domino Logic – Place static inverter on gate output



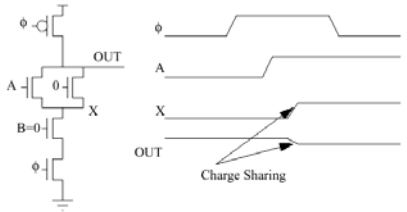
Static inverter on output ensures that inputs to cascaded gates follow monoticity rule: inputs either remain high or make single transistion low to high.

Domino Logic can only implement Non-inverting functions



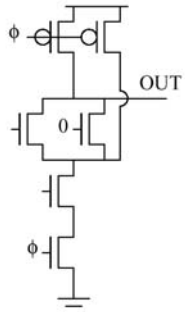
Can't do this because Y will high during precharge. If goes to another Domino input, will corrupt it.

Charge Sharing



X is an intermediate node which is low during precharge. When A goes high, but B remains 0, charge is distributed between output node and node X. If capacitance at intermediate node X is large enough (depends on complexity of circuit), OUT can drop enough to viewed as a '0'.

Secondary Precharge Transistor

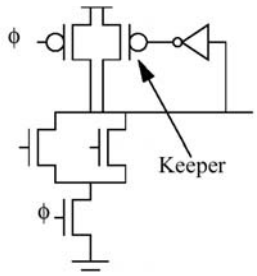


Extra precharge transistor added for precharging internal nodes. Rule of thumb is to precharge every other level of the N-tree. Extra precharge transistors add more diffusion capacitance with N-tree, slowing performance.

Subthreshold Leakage

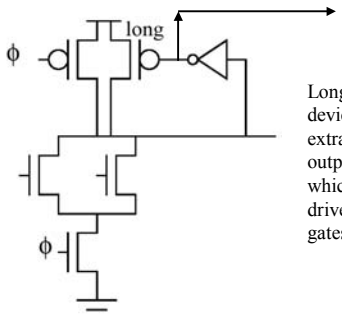
- If the clock stays high for an extended period, the output charge will leak off due to subthreshold currents
- Dynamic circuits typically have a minimum clock frequency requirement because of this.
- Subthreshold leakage gets worse as you scale down in technology.

Weak Keeper



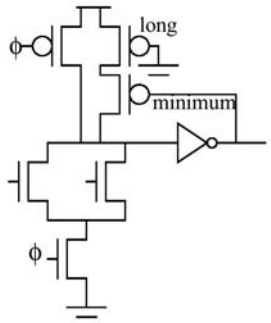
This will slow the circuit operation because the PMOS keeper will fight the evaluation. Must make the PMOS keeper weak.

Long Channel Keeper



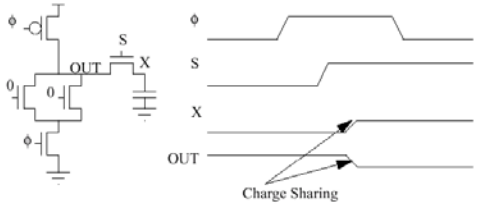
Long channel device presents extra load to output inverter, which has to drive other gates.

Split Keeper



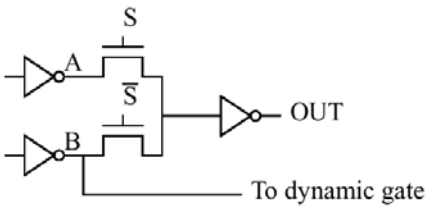
Keeper gate load now reduced on gate output.

Charge Sharing with Pass Transistors



If S turns on during evaluation, charge at Node X can corrupt charge on dynamic gate.

Glitching via Pass Transistors



If S and S' are on at the same time for a short period of time, nodes A, B can fight each other causing a glitch, which then could trigger a dynamic gate. Dynamic gate inputs are sensitive to glitches.

Performance Considerations

Critical path is determined by pulldown speed of NTREE + pullup speed of inverter (Inverter Tplh). Only need to optimize the Tplh of the inverter.

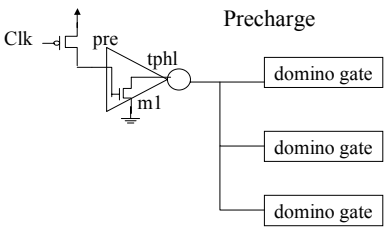
During evaluation, cascaded domino gates trigger sequentially via 0 to 1 transistions. Length of precharge period will be set by delay along longest path in the domino logic (critical path).

During precharge, all domino gates precharge in parallel.

Precharge time is not equal to Evaluate time, clock does not to be a 50% duty cycle clock (but probably is in a pipelined system)

Precharge period must be long enough so that inverter 1 to 0 transistion reaches all its fanins. Size of the precharge transistor + tphl of inverter should be sized to meet precharge period.

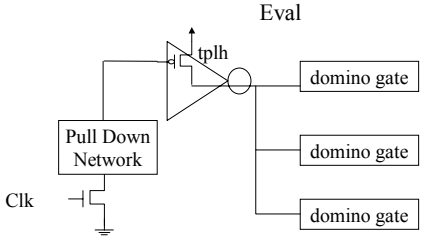
Precharge



Path through *pre*+m1 sized to meet minimum precharge period requirements.

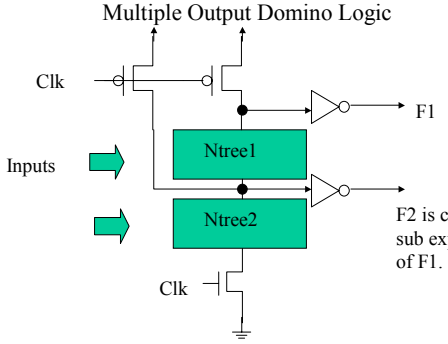
Don't want to make *pre* too large because of clock loading. Don't want to make m1 too large because will load 'evaluation' path.

Eval



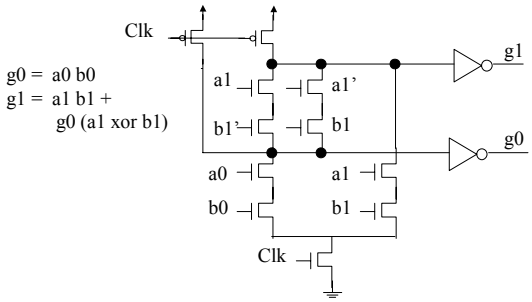
Need to optimize tplh path in inverter. Want to size the EVAL path first, then size the precharge path. If using a 50% duty cycle clock, eval time will be longer than precharge time, and will size precharge path to be equal to eval time.

Multiple Output Domino Logic

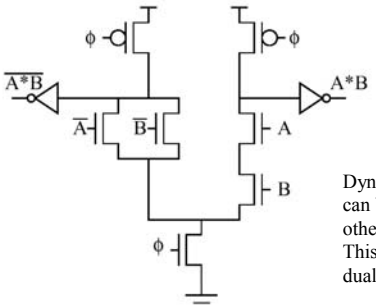


Carry Lookahead logic

g0 = a0 b0
g1 = a1 b1 +
g0 (a1 xor b1)

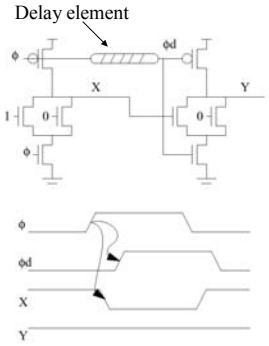


Dynamic DCVSL



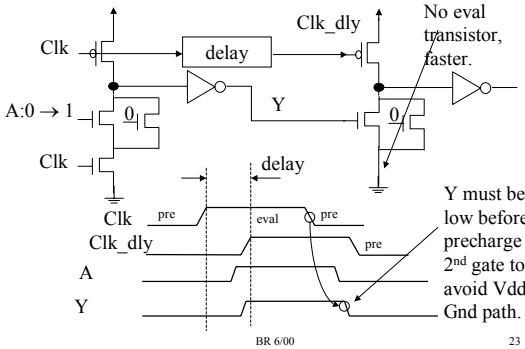
Dynamic techniques can be applied to other circuit families. This is also known as dual rail domino.

Self Timed Domino



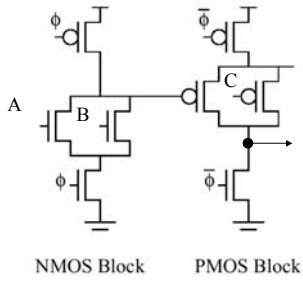
Delay element delays clock to next gate. Delay time must allow first gate outputs to settle after evaluation. Removes inverter delay between static gates.

Self Timed Domino, Variation #2



Y must be low before precharge of 2nd gate to avoid Vdd to Gnd path.

Other Dynamic Styles - NORA (NP-CMOS)

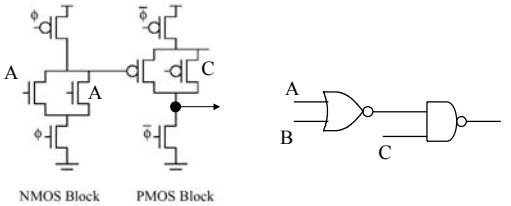


Alternate gates with Pulldown networks (PDNs) with gates that have Pullup networks (PUNs).

PUNs gates must have inputs from PDN gates, PDN gates must have inputs from PUN gates. No inverter between gates needed.

NORA (NP-CMOS)

NMOS gates evaluate when Clock is high, PMOS gates evaluate with Clock low. Can implement inverting logic.



Principle disadvantage is low noise margins. High margin is Vtp, Low margin is Vtn.