Papers to be used for Final Exam (cont)

A third-generation SPARC V9 64-b microprocessor
Heald, R.; Aingaran, K.; Amir, C.; Ang, M.; Boland, M.; Dixit, P.; Gouldsberry, G.; Greenley, D.; Grinberg, J.; Hart, J.; Horel, T.; Wen-Jay Hsu; Kaku, J.; Chin Kim; Song Kim; Klass, F.; Kwan, H.; Lauterbach, G.; Lo, R.; McIntyre, H.; Mehta, A.; Murata, D
Solid-State Circuits, IEEE Journal of , Volume: 35 Issue: 11 , Nov. 2000
Page(s): 1526 -1538

A 16-Mb 400-MHz loadless CMOS four-transistor SRAM macro
Takeda, K.; Aimoto, Y.; Nakamura, N.; Toyoshima, H.; Iwasaki, T.; Noda, K.; Matsui, K.; Itoh, S.; Masuoka, S.; Horiuchi, T.; Nakagawa, A.; Shimogawa, K.; Takahashi, H.
Solid-State Circuits, IEEE Journal of , Volume: 35 Issue: 11 , Nov. 2000

A 1.0-GHz single-issue 64-bit powerPC integer processor
Silberman, J.; Aoki, N.; Boerstler, D.; Burns, J.L.; Sang Dhong; Essbaum, A.; Ghoshal, U.; Heidel, D.; Hofstee, P.; Kyung Tek Lee; Meltzer, D.; Hung Ngo; Nowka, K.; Posluszny, S.; Takahashi, O.; Vo, I.; Zoric, B.
Solid-State Circuits, IEEE Journal of , Volume: 33 Issue: 11 , Nov. 1998
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Papers to be used for Final Exam

Fast low-power decoders for RAMs
Amrutur, B.S.; Horowitz, M.A.
Solid-State Circuits, IEEE Journal of , Volume: 36 Issue: 10 , Oct. 2001
Page(s): 1506 -1515

The future of wires
Ho, R.; Mai, K.W.; Horowitz, M.A.
Proceedings of the IEEE , Volume: 89 Issue: 4 , April 2001
Page(s): 490 -504

Topics from Papers

- Clocking/Logic styles used for Power PC, Sparc V9
- Self-resetting Domino logic style used in low-power RAM decoders – how does it work? Advantages? Disadvantages? Why is interesting for RAM decoders?
- 4-transistor loadless SRAM cell – why is this interesting? What is it?
- Wires – scaling, inductive effects, implications for future architectures, CAD tools.