## IA-64 CPU and Clk Design

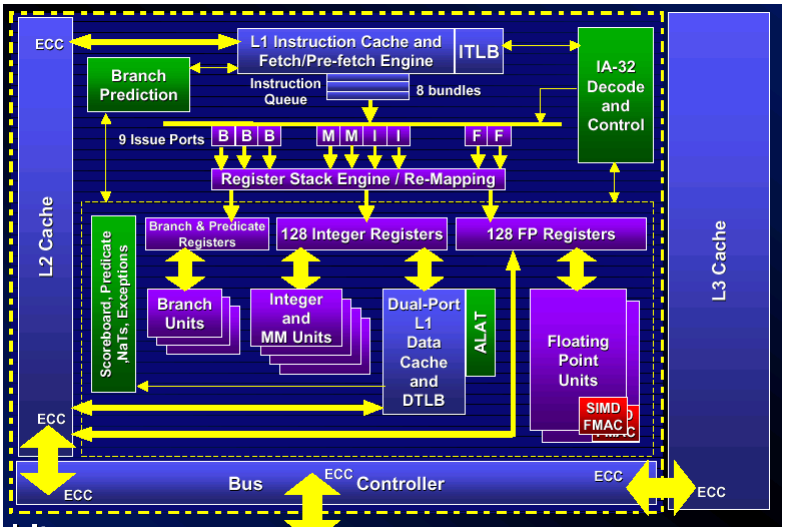
- This lecture uses two papers that discuss the evolution of the Alpha CPU and clocking strategy over three CPU generations
  - Tam, S. et.al, "Clock Generation and distribution for the First IA-64 microprocessor", IEEE Journal of Solid State Circuits, Vol 35, Issue 11, Nov 2000.
  - Rusu, S. and Singer G, "The first IA-64 microprocessor ", IEEE Journal of Solid State Circuits, Vol 35, Issue 11, Nov 2000.
- All notes in this lecture are from these two papers.



## The IA-64

- IA-64 ISA is successor to the Pentium 4, which was the successor to the Pentium 3/2/1.
  - 64-bit architecture, all registers 64-bits wide
  - 128 General Registers, 128 Floating Point Registers
  - G0-G31 are global registers, G32-G127 are part of the "Register Stack" where a dynamic number of them can be allocated as part of procedure call/return and be visible to only that procedure (similar to Sparc register windows).
  - Superscalar, maximum issue of 6 instructions per clock
  - Supports both speculative branching and speculative loading
- *Itanium* is the first implementation of the IA-64 ISA.
  - Executes x86 code (IA-32) with a separate execution engine.

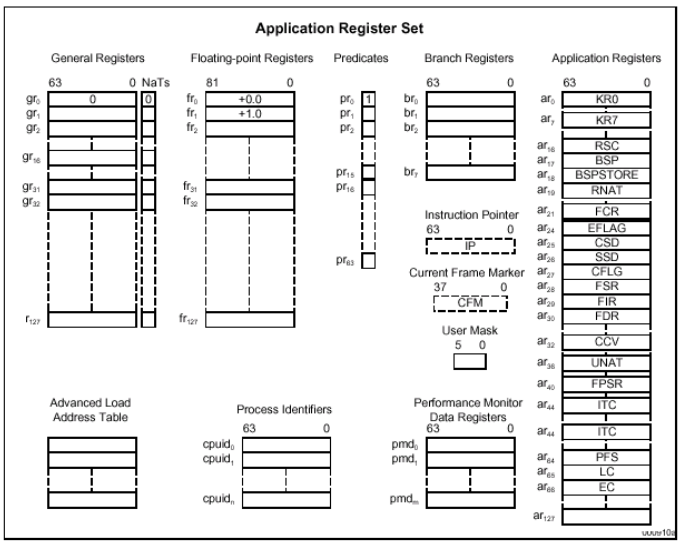
## Itanium Block Diagram






## Register Set (Integer RF has 8 read ports, 6 Write ports)

Figure 3-1. Application Register Model



# Technology

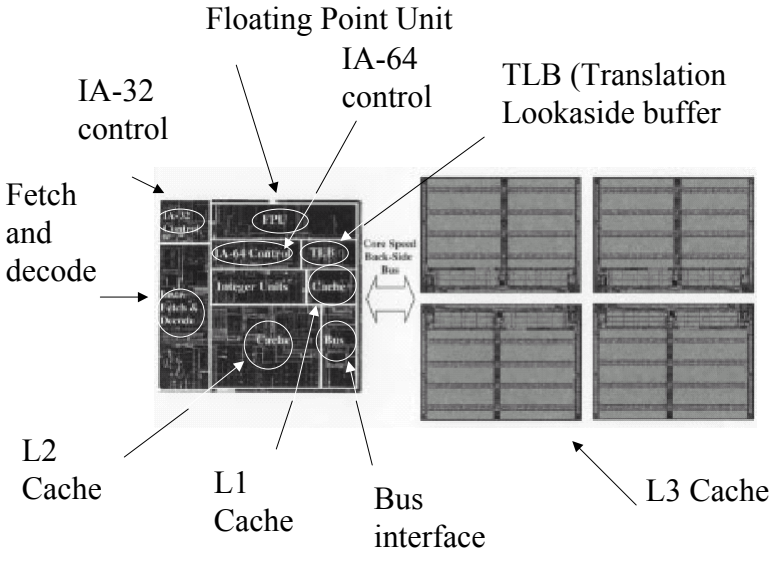
- 0.18µ CMOS
- 25.4 million transistors
- 6 metal layers
- Flip-chip with 1014 pads

Recall that the Alpha had 21264 had 15.2 million transistors

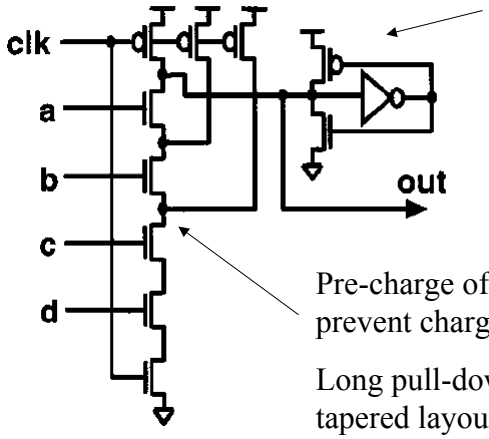
TABLE I
0.18-$\mu$m PROCESS FEATURES

| Layer | Pitch |
|---|---|
| Poly | 0.48µm |
| Metal 1 | 0.60µm |
| Metal 2 | 0.72µm |
| Metal 3 | 0.72µm |
| Metal 4 | 1.45µm |
| Metal 5 | 1.80µm |
| Metal 6 | 2.00µm |





## IA-64 Logic Design – 4-phase Domino



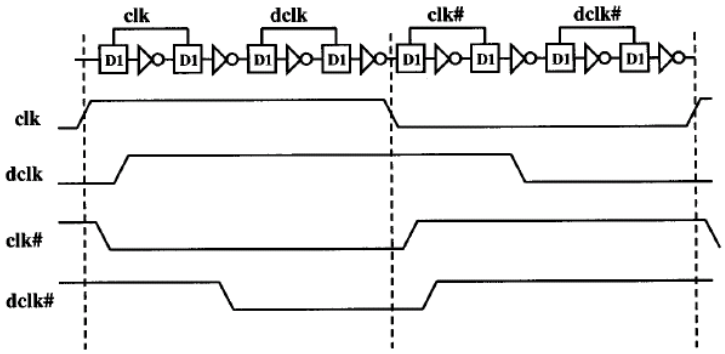

Full keeper to support clock stopping. All circuits had full or half keepers.

Pre-charge of internal nodes to prevent charge sharing

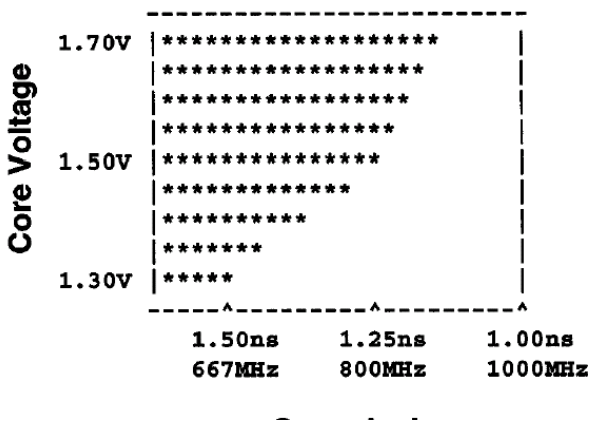
Long pull-down stacks used tapered layout to reduce source/drain capacitance



## 4-Phase Clocking



## Schmoo Plot of Operation




A schmoo plot shows Voltage vs. Frequency operation – '*' indicates operation at that Voltage, Frequency

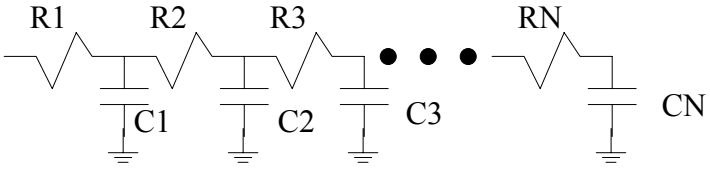


## Power Distribution

- Used M5/M6 grid
- 800 nf of on-chip decoupling capacitors
- Additional on-package decoupling capacitors

## Repeater Insertion

Recall RC wire delay analysis



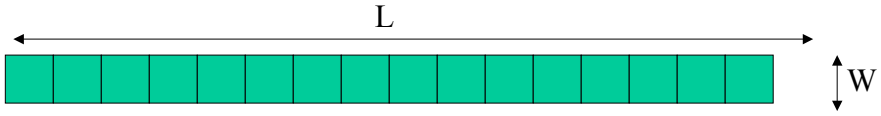

A wire is a distributed RC line

One estimate of the wire delay is $0.9 * R_{tot} * C_{tot}$ where $R_{tot}$ and $C_{tot}$ is the lumped Resistance/Capacitance of the wire (the sum of all of the R's, C's) (Rabaey, Table 8.10, pg 472).

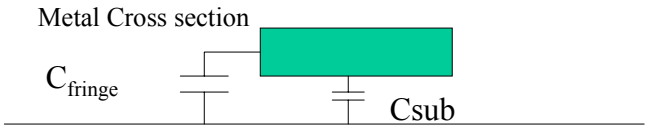
This estimation is the 10% to 90% delay of the wire – the delay measured from the 10% point on the input waveform to the 90% point on the output waveform



## Wire RC Calculations




$R_{wire} = R_{sq} * L / W$



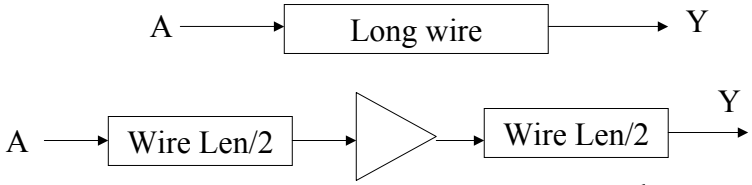

Cwire = Cfringe *Length + Csub * Length *Width

## Reducing Wire Delay of Long Wires

Can reduce wire delay by making wire wider if fringing capacitance dominates wire capacitance.

If substrate capacitance dominates, then increasing width decreases R, but also increases C by same amount so total RC remains the same.

Can also reduce wire delay by splitting a wire into segments and putting a buffer between each segments.



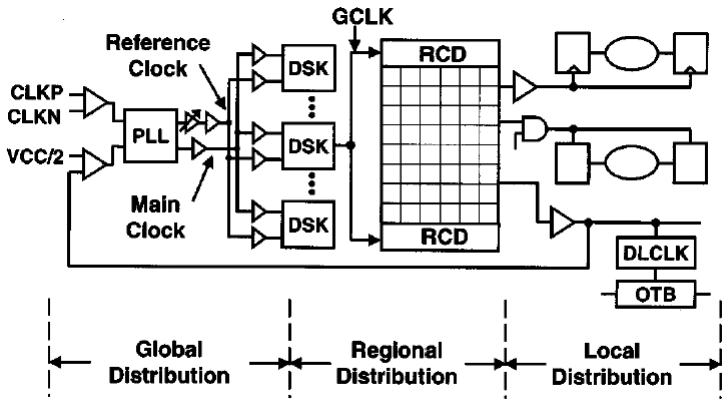

If wire is long enough, and buffer fast enough, 2nd configuration will have less delay.



## Automated Buffer Insertion

- Of 13000 nets routed at top level of processor, 11000 required buffer insertion because delay was dominated by RC
- 45 repeater stations distributed evenly in routing channels across die
  - Special repeater cells had integrated decoupling capacitors
- Repeater insertion flow fully automated an integrated with logic, floorplan, layout, and timing verification environments

# IA-64 Clock Distribution

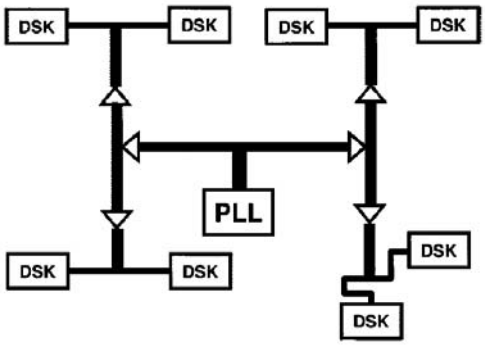



DSK – deskew buffers, RCD – Regional Clock Distribution Network



# Reference, Core clocks

- On chip PLL generated 2X reference clock which is then divided by two to form a 50% duty cycle core clock
  - External clock (system clock) is input to PLL
- Both 2X reference clock and core clock is distributed across die via an H tree




Routed in M5/M6

Fully laterally shielded with Vss/VDD

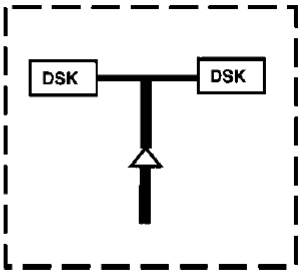
Inductive reflections minimized at branch points by sizing wires to match impedances

## Inductance Affects Delay

Delay in Clock distribution metal H-tree network affected by R, C, and L.

For Ghz speed clocks in a metal distribution network, must include L in delay calculations

| RLC and Return Path Extraction | Line Delay | Gate Delay |
|---|---|---|
| Addition of return path resistance | + 27 % | - 3% |
| Addition of Inductance | + 8 % | -10 % |
| Difference from RC Model | + 35 % | - 13% |

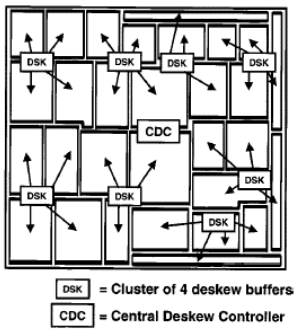



Inductance adds extra delay in current return path
Inductive effects decreased clock buffer delays dues to faster transition rates.



## Regional Clock Distribution

- De-skew buffers (DSK), Regional Clock Drivers (RCD), and Region Clock Grid (RGD)
- 30 clock regions serviced by regional clocks
- Regional Clock Grid implemented in M4, M5
  - Floats over one or more functional units
  - Full lateral shielding via Vss/Vdd



# Alpha vs IA64 Approach

- Alpha CPU Major Clock = IA 64 Regional clocks
  - Alpha did not attempt to deskew Major clocks with GCLK
  - Alpha used local clocks generated from major clocks and did timing analysis, path delay matching between clocks and data to solve timing problems
- This does NOT account for delays due to on die process variations
  - At Ghz clock speeds, skew due to on die process variations can cause timing failures
- IA64 used an 'active' distributed deskewing approach for GCLK and Regional Clocks
  - Wanted to avoid the detailed delay matching, timing analysis required in the Alpha design after complete implementation because of impact on design schedule
  - Account for delay due to on die process variations



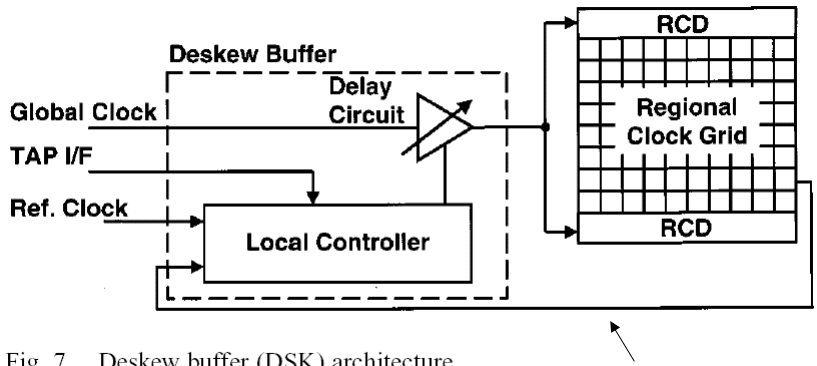



Fig. 7. Deskew buffer (DSK) architecture.

Delay circuit used to control edge alignment of Global clock with Regional Clock.

In general, this is a form of a Digital Delay Locked Loop (DLL).

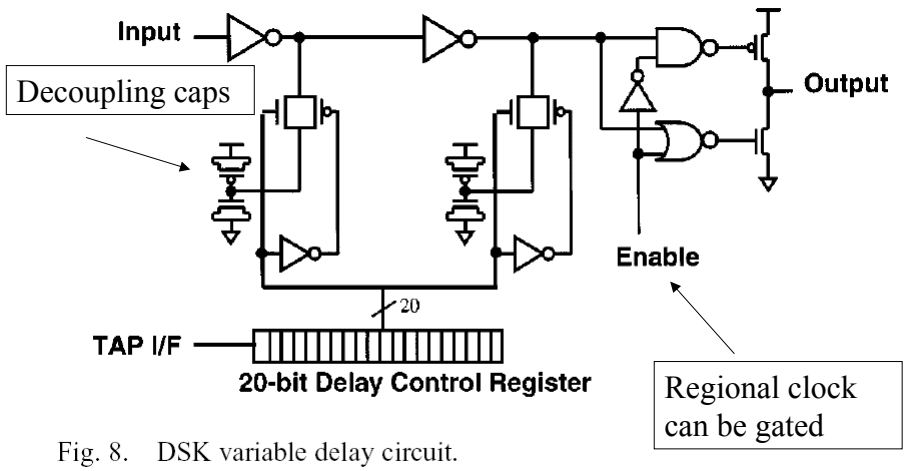



Fig. 8. DSK variable delay circuit.

Shifting a '1' from one end decreases delay, shifting a '0' from opposite end increases delay.

Delay range was 170 ps in 8.5 ps steps. Phase adjustments made every 16 clock cycles.



## Controller for Deskew Buffer Register

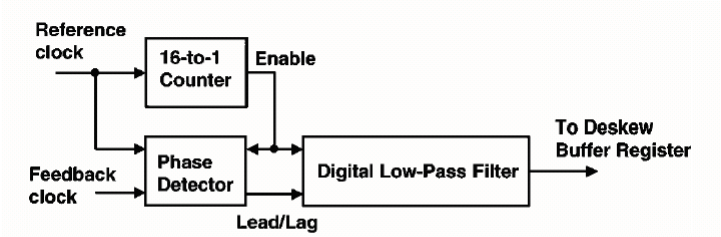



Fig. 9. Deskew buffer local controller.

Deskew Register adjusted every 16 clock cycles of Reference Clock.

The Deskew buffer is just a simple form of a Delay Locked Loop (DLL).

## Why a Reference Clock?

- The goal of the DSK was to deskew the global (core) clock with respect to the regional clocks
  - Reference clock was 2X core clock
  - Regional clocks were simply a delayed version of the global clock
  - Reference clock was not deskewed but smaller distribution region and more balanced routing gave less skew in reference clock.
- Not possible to maintain a balance routing network and load matching for core clock over such a large design with multiple design teams since the core clock was driving logic
  - However, it was possible to design balanced routing network and have load matching for the reference clock since all it drove were the DSK's and global clock design team solely responsible for reference clock design
  - Feedback clocks from the regional clock distribution were then used to deskew regional clocks with respect to reference clock.



## Skew Elements

- Total skew of design based on residual skew in reference clock, uncertainty of phase detector in DSK, and mismatches of feedback clocks
  - Reference clock did not have as large a distribution region as the core clock, and loads were better matched, so had tighter skew than would have been possible with global clock
  - Feedback clock routes were kept short with respect to DSKs
  - Phase detector uncertainty kept small via symmetric layout techniques and by allowing a long time for phase comparison
- Achieved maximum skew was 28 ps (2.8% of a 1 Ghz clock period).

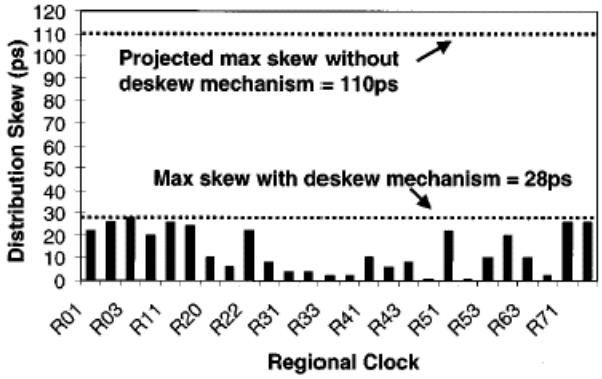


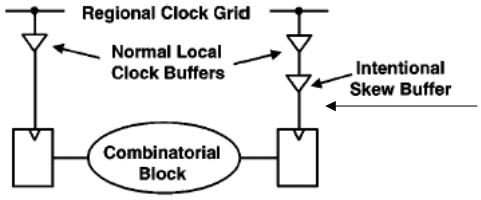

Fig. 10. Experimental skew measurements.

Measured skew via Laser voltage probing



# Local Clocks

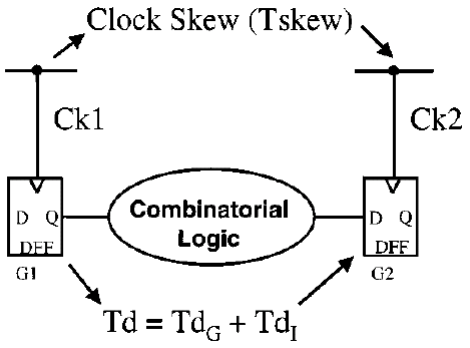
- Local clocks generated from Regional Clocks and provided clocks needed by domino logic
- Full timing analysis performed on local clocks
- Local clocks responsibility of functional block design teams
- Global and regional clock responsibility of global clock design team




Delay added for time borrowing or to account for skew in local clock

Fig. 6. Local clock distribution.

## Hold Time Analysis (another look)




$Td_I$ includes delay through combinational logic plus hold time on G2

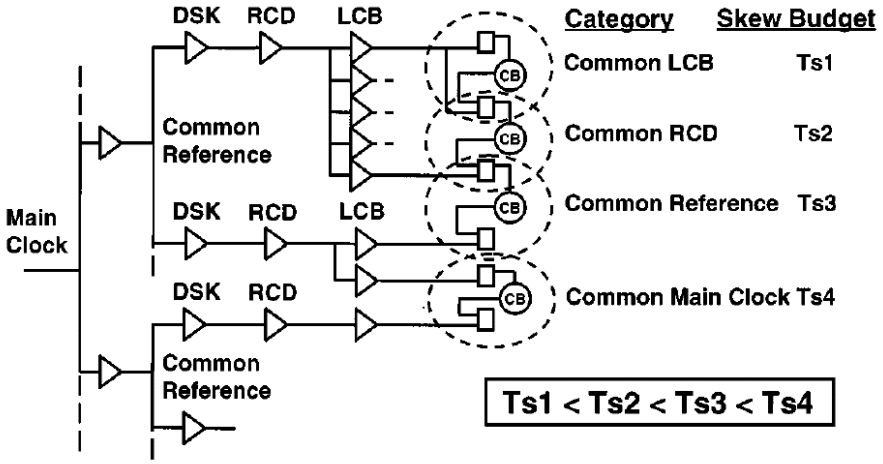
This was called 'race analysis' in Alpha notes

Min(Td) ≥ max (Skew)

If shortest path from G1 to G2 is less than max Skew, than incorrect value may get clocked into G2 when clock edge arrives at G2.



## Four different cases for Max(skew)

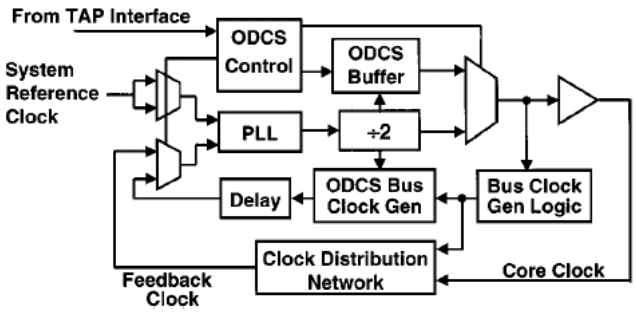



LCB = local clock buffer.
Common reference means in same DSK cluster

## On-Die-Clock-Shrink Block

Because of Ghz clock rate, no tester able to accurately supply and manipulate clock edges if PLL bypassed.

Functional block called On-Die-Clock-Shrink (ODCS) block included for edge manipulation for post silicon debug.






## ODCS Features

Could shrink low/high phase of clock cycle-to-cycle

Range was 200 ps in 14 linear steps.

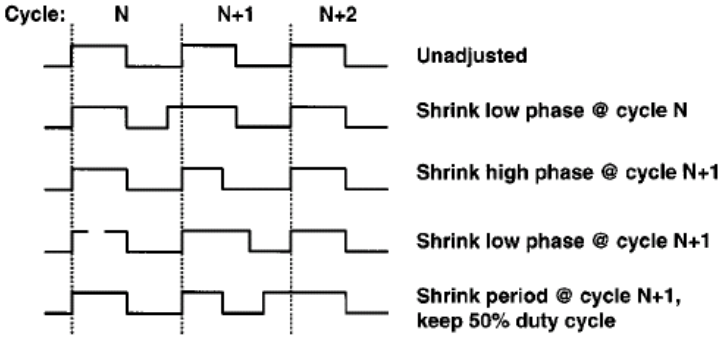



Fig. 16. ODCS capabilities.