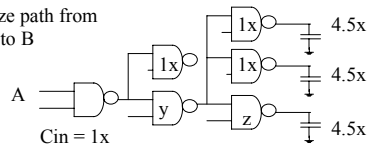
Branching Effort revisited

This time, do NOT size off path load with on path load. Load measured in 2-input Nands

Size path from A to B



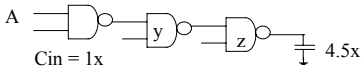
Path logic effort G = g0 * g1 * g2 = 4/3 * 4/3 * 4/3 = 2.37
Branch effort, 1st stage = (y+1)/y = b1
Branch effort, 2nd stage = (z + 2)/z = b2

Path Branch effort B = (y+1)/y * (z+2)/z (no closed form!)
Path electrical effort H = Cout/Cin = 4.5C/C = 4.5
Path stage effort = F = G*B*H = 2.37*4.5*B = 10.7*B

Min delay = $N(F)^{1/N} + P = 3*(10.7 * b1*b2)^{1/3} + 3(2pinv)$

First, ignore branching contribution

Size path from A to B



Path logic effort G = g0 * g1 * g2 = 4/3 * 4/3 * 4/3 = 2.37

B = 1
Path electrical effort H = Cout/Cin = 4.5C/C = 4.5
Path stage effort = F = G*B*H = 2.37*4.5 = 10.7

Min delay = $N(F)^{1/N} + P = 3*(10.7)^{1/3} + 3(2pinv) = 12.6$

Size gates

Stage effort of each stage should be:
f(min) = $(F)^{1/N} = (GBH)^{1/N} = (10.7)^{1/3} = 2.2$

Determine Cin of last stage:

Cin(z) = g * Cout / f(min) = 4/3 * 4.5 / 2.2 = 2.7

Determine Cin of middle stage:

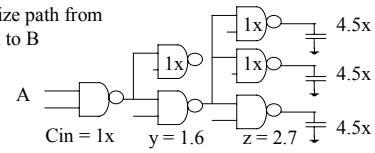
Cin(y) = g * (Cin(z))/ f(min) = 4/3 * (2.7) / 2.2 = 1.6

Is last stage correct?

Cin(A) = g * (Cin(y))/ f(min) = 4/3 * (1.6) / 2.2 = 1

Recompute Delay with sizes

Size path from A to B



Path logic effort G = g0 * g1 * g2 = 4/3 * 4/3 * 4/3 = 2.37
Branch effort, 1st stage = (1.6+1)/1.6 = 1.6
Branch effort, 2nd stage = (2.7+2)/2.7 = 1.7

Path Branch effort B = 1 * 1.6 * 1.7 = 2.7
Path electrical effort H = Cout/Cin = 4.5C/C = 4.5
Path stage effort = F = G*H*B = 2.37*4.5*2.7 = 29

Min delay = $N(F)^{1/N} + P = 3*(29)^{1/3} + 3(2pinv) = 15.2$

Resize gates

Stage effort of each stage should be:
f(min) = $(F)^{1/N} = (GBH)^{1/N} = (29)^{1/3} = 3.1$

Determine Cin of last stage:

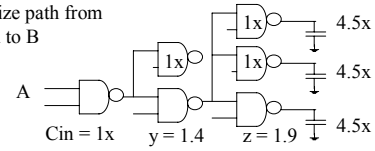
Cin(z) = g * 1 *Cout / f(min) = 4/3 *1 * 4.5 / 3.1 = 1.9

Determine Cin of middle stage:

Cin(y) = g * (b2 *Cin(z))/ f(min) = 4/3 * 1.7 *1.9/ 3.1 = 1.4

Recompute Delay with sizes

Size path from A to B



Path logic effort G = g0 * g1 * g2 = 4/3 * 4/3 * 4/3 = 2.37
Branch effort, 1st stage = (1.4+1)/1.4 = 1.7
Branch effort, 2nd stage = (1.9+2)/1.9 = 2.1

Path Branch effort B = 1 * 1.7 * 2.1 = 3.6
Path electrical effort H = Cout/Cin = 4.5C/C = 4.5
Path stage effort = F = G*H*B = 2.37*4.5*3.6 = 38

Min delay = $N(F)^{1/N} + P = 3*(38)^{1/3} + 3(2pinv) = 16.1$

Resize gates

Stage effort of each stage should be:
$f(min) = (F)^{1/N} = (GBH)^{1/N} = (38)^{1/3} = 3.4$

Determine Cin of last stage:

$Cin(z) = g * 1 * Cout / f(min) = 4/3 * 1 * 4.5 / 3.4 = 1.8$

Determine Cin of middle stage:

$Cin(y) = g * (b2 * Cin(z)) / f(min) = 4/3 * 2.1 * 1.8 / 3.4 = 1.5$

Summary of Iterations

Iteration #	1st Stage Size	2nd Stage Size
1 (ignore branching)	1.6	2.7
2	1.4	1.9
3	1.5	1.8