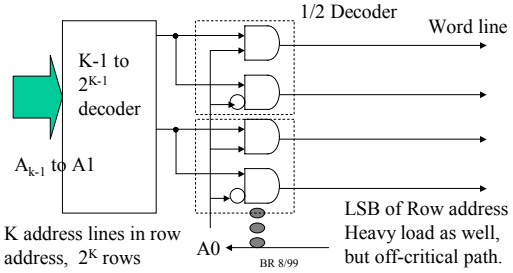
Word Line Driver

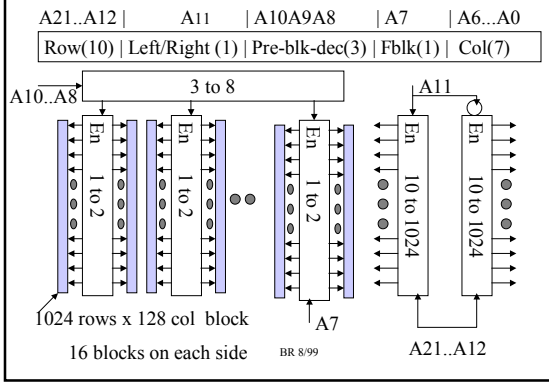
Last stage of row decoding typically decodes only 1-address line (1/2 decoder) because the final stage must be sized to drive the word line load (word-line driver).



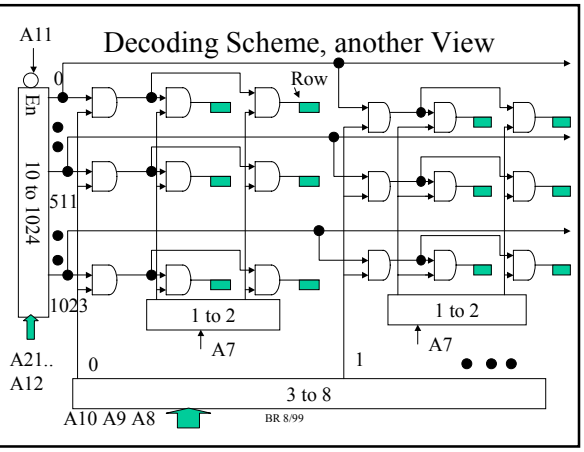
Mitsubishi 4 Mbit SRAM

- 4Mb x 1, 2^{22} bits, 22 address lines
- A single square array would be 2^{11} rows x 2^{11} columns, each word line would have 2048 RAM cell loads!!
- Use hierarchical decoding to break large array into smaller arrays
- Use 32 blocks
  - Each block is 1024 rows x 128 columns = 128Kb
  - 128Kb x 32 = 2^{17} x 2^5 = 2^{22} = 4 Mb.
  - 7 bits for column decode (128 columns). Remaining bits (15) for block (5), row decode (10).

Decoding Scheme



Decoding Scheme, another View



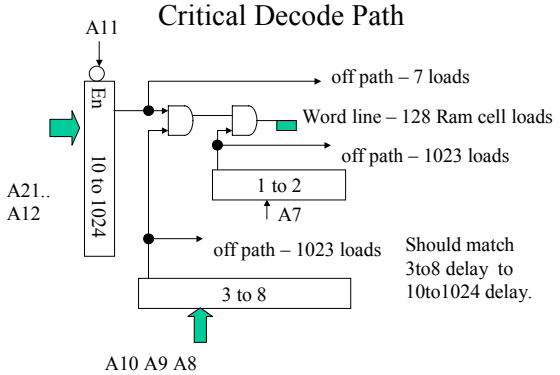
Loading

- On 10 to 1024 decoder outputs
  - 8 loads (16 blocks divided into 8 groups of 2)
- On 3 to 8 decoder outputs
  - 1024 loads
- On 2 to 1 decoder outputs
  - 1024 loads

Want to equalize delay paths:

complex decode + light load = small decode + large load
10 to 1024 8 loads = 3 to 8 1024

Critical Decode Path

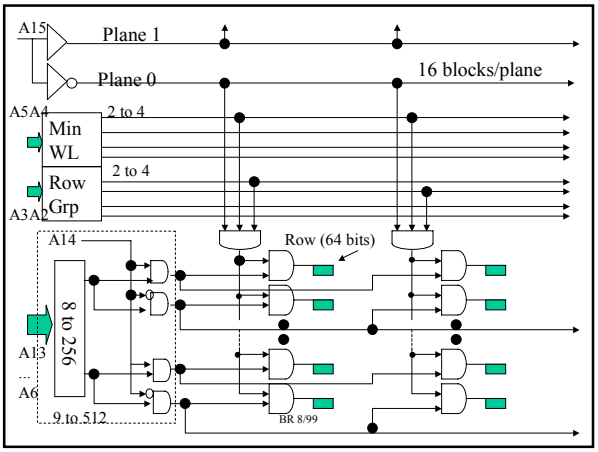


Cypress 1 Mb Dual Port RAM

- Arranged 64K x 16
- Array split into 32 blocks, each 512 rows by 64 bits (4 words of 16)
  - 16 sense amps per block, 1 sense amp per bit shared among 4 words
  - 32 blocks x 512 rows x 64 bits = 2^5 x 2^9 x 2^6 = 2^{20}.

Plane(1)	Max WL(9)	Min WL(2)	Row Grp(2)	Col(2)

A15 | A14..A6 | A5A4 | A3 A2 | A1..A0



Loading

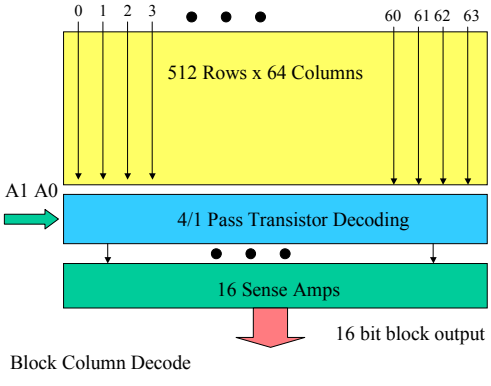
- on 8 to 256 decoder output (2 loads)
- on A14 (512 loads)
- on 9 to 512 decoder outputs (16 loads)
- on 4 to 16 decoder (combined Min WL + Row Grp)
  - 512 loads
- On final wordline driver output (64 SRAM loads)

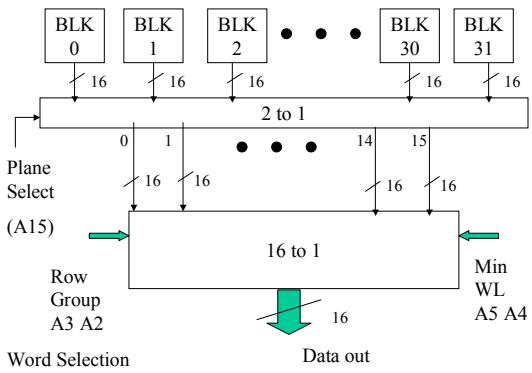
Delays:

Want Dx = 8 to 256 decoder = A14 (512 loads)
Want Dy = 4 to 16 decode (512 loads) = 9 to 512 (64 SRAM bit loads)

Misc Comments

- The plane bit is not involved in the Major Word line decoding.
  - Both Major Row decoders active but still only one final word line is active
- Physical layout had Row Group and Min WL lines running down the center of the chip with planes on left/right side

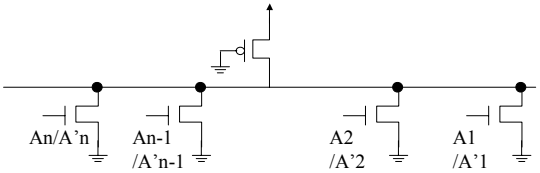




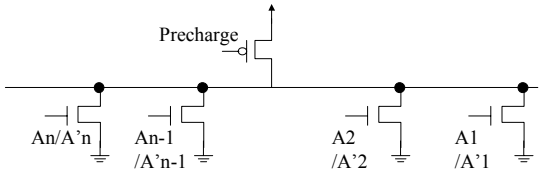
Fast Decoders

Need Fast, Wide Decoders for Row Decode.

Because of large number of inputs, use a NOR form with a static pullup or precharged pullup.

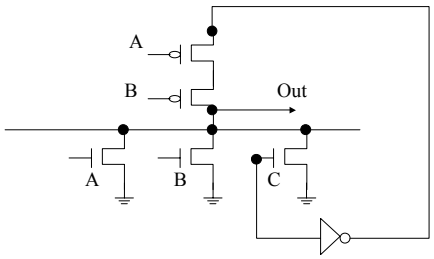


Fast Decoders (cont)



Precharge can be generated from clock or address transition detection logic.

Power Decoded NOR



A NOR gate version that saves power.