Inverter Delay Scaling

Scale Factor				2.7		2.4	
		Agilent		HP		Leda	
Times in ps		1.6		0.6		0.25	
		tphl	tplh	tphl	tplh	tphl	tplh
measured		1370	1430	186	173	67	75
scaled (long channel)				192.7	201.1	32.3	30.0
%diff				-4%	-16%	52%	60%
scaled (short channel)				513.8	536.3	77.5	72.1
%diff				-176%	-210%	-16%	4%

Long channel scaling from 1.6 to 0.6

Short channel scaling from 0.6 to 0.25

Complex Gate Delay Scaling

Scale Factor			2.7		2.4	
	Agilent		HP		Leda	
Times in ps	1.6		0.6		0.25	
	tphl	tplh	tphl	tplh	tphl	tplh
measured	1190	2050	274	294	122	160
scaled (long channel)			167.3	288.3	47.6	51.0
%diff			39%	2%	61%	68%
scaled (short channel)			446.3	768.8	114.2	122.5
%diff			-63%	-161%	6%	23%

Long channel scaling from 1.6 to 0.6

Short channel scaling from 0.6 to 0.25

Inverter Effective Capacitance Scaling

Scale Factor				2.7		2.4	
		Agilent		HP		Leda	
Cap values in fF		1.6		0.6		0.25	
		noload	loaded	noload	loaded	noload	loaded
measured		9.6	42	4.9	18	3.6	14
scaled				3.6	15.8	2.0	7.5
%diff				27%	13%	43%	46%

Scaling prediction a bit low from 1.6 to 0.6

Scaling prediction ½ actual value

Complex Gate Effective Capacitance Scaling

Scale Factor				2.7		2.4	
		Agilent		HP		Leda	
Cap values in fF		1.6		0.6		0.25	
		noload	loaded	noload	loaded	noload	loaded
measured		33	65	13	27	10	19
scaled				12.4	24.4	5.4	11.3
%diff				5%	10%	46%	41%

Scaling prediction ok from 1.6 to 0.6

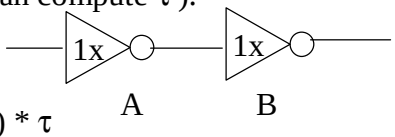
Scaling prediction ½ actual value

Why is Scaling Prediction too low for Capacitance?

- In sub-micron, short circuit currents become a larger factor.
  - Not included in scaling factor that is applied to physical capacitance
- This contributes to power dissipation, which leads to larger effective capacitance than what is predicted by scaling of physical capacitance

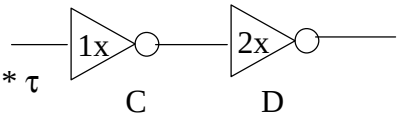
The Parasitic Delay *p*

- Note that the parasitic delay (no-load) *p* is a constant and independent of transistor size; as you increase the transistor sizes the capacitance of the gate/source/drain areas increase also which keeps no-load delay constant
- To measure P (once P is known, can compute τ).



$A\_delay = (g*h + p) * \tau = (1*1 + p) * \tau$

$\tau = (A\_delay)/(1+p)$



$C\_delay = (g*h + p) * \tau = (1*2 + p) * \tau$

$C\_delay = (2+p)\ (A\_delay)/(1+p)$

$p = (2*A\_delay - C\_delay)/\ (C\_delay - A\_delay)$

P measurements for Inverter

Gvalue for inverter	1.0			
Size	1	2	4	6
PMeasurements	1X load	2X load	4x load	6xload
	64.0	72.0	90.0	107.0
P calculate		7.0	6.4	6.4
Tau		8.0	8.7	8.6

Used three different loads (2x, 4x, 6x) to measure P.

Average of P values: 6.6
Tau value: 8.4

P measurement for Nand2, Nor 2

Size	Inverter	Nand2	Nor2
1x	52.0	87.0	91.0
2x	53.0	86.0	95.0
4x	53.0	86.0	96.0
8x	52.0	85.0	96.0
Avg.	52.5	86.0	94.5
Ratio to Inverter		1.6	1.8
Calculated P based on Pinv.noload		10.8	11.9

Calculated P based on noload ratio of Nand2, Nor2.

I.e. Pnand2 = Pinv * (Nand2_noload/Inv_noload)

Note that no-load delays are independent of gate size.

Delay Prediction using Logical Effort Model

nand2	1X load	2X load	4x load	6xload
Measured	99.0	111.0	135.0	156.0
Calculated	103.6	114.8	137.2	159.6
% diff	4.6%	3.4%	1.6%	2.3%

nand2 driving 1X, 2X, 4X, 6X nand2 loads.

Example Calculation for 4X load:

delay = (g*h + Pnand2) = 4/3* Cout/Cin + Pnand2
= 4/3* 4/1 + Pnand2

Delay Prediction using Logical Effort Model

Nor2	1X load	2X load	4x load	6xload
Measured	116.0	135.0	170.0	206.0
Calculated	114.8	128.8	156.8	184.8
% diff	-1.0%	-4.6%	-7.8%	-10.3%

nor2 driving 1X, 2X, 4X, 6X nor2 loads.

Example Calculation for 4X load:

delay = (g*h + Pnor2) = 5/3* Cout/Cin + Pnor2
= 4/3* 4/1 + Pnor2