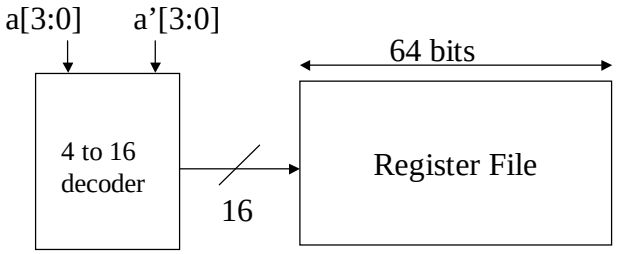
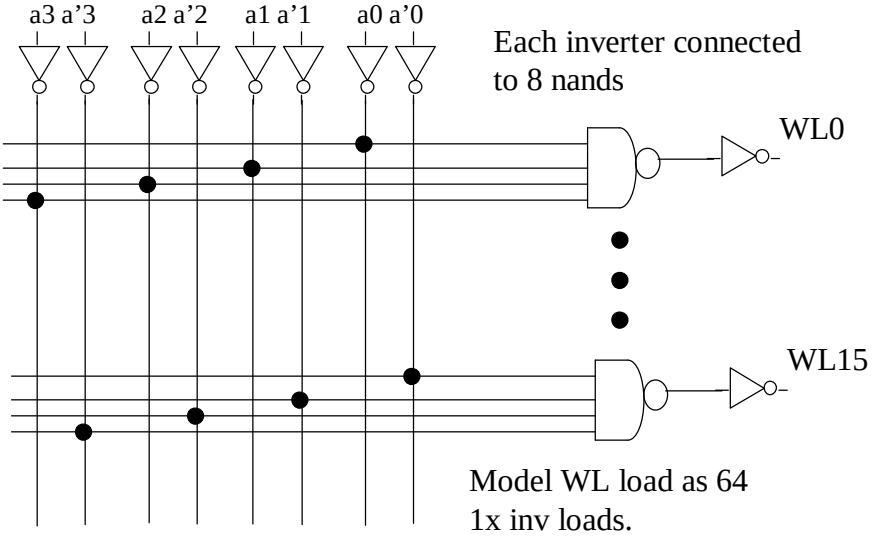
Problem #1: Sizing Problem



16 x 64 register file

Decoder



Problem Statement

- Using the logical effort model, determine ‘p’, tau for a 4-input nand using Leda 0.25u process, Vdd = 2.5 v.
- Size the inverters, nand gate in the previous slide using the logical effort model.
- Predict the delay, and then compare simulated delay to predicted delay.

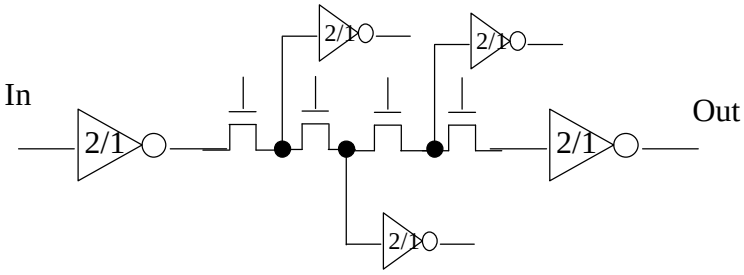
Problem #2

a. Find the inverter size that will give equal rise/fall delay when driving a 1X load for the specified technology/Vdd.

b. For a string of 9 inverters driving NO LOAD, compare via simulation the average delay using the inverter sized in part (a) and to the delay of a string of inverters whose size is the square root of the size found in (a).

Problem #3

For the problem below, determine via simulation if progressive sizing or uniform sizing of pass transistors yields minimum delay. Note that last inverter has no load. Limit NMOS pass size to 4x size.



Problem #4

Implement the function:

F = (A and not(B) and not(C)) or (not(A) and C and D)

in DCVSL. Use the minimum number of transistors.

Assume A,B,C,D and their complements are available.