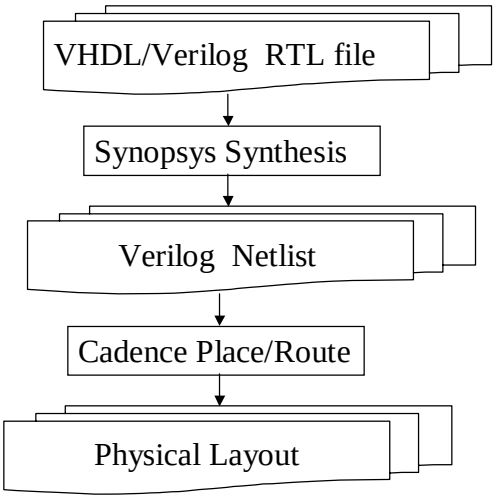
EE 8273 Project

- Create a minimum standard cell library for the Synopsys/Cadence toolsets
- Requirements
  - Minimum standard cell library – nand2, nor2, not, dffsr (dff with reset and preset), logic0 (pulldown), logic1 (pullup)
  - IO – vddpad, gndpad, in pad, out pad (no tristate)
  - Demonstrate design methodology that includes VHDL/Verilog RTL specification to physical layout

Methodology



Requirements for Synthesis

- Standard cells and IO cells must be characterized for delay
  - Delay model must use 2-d lookup table based on input slope and output capacitance load
    - Must be at least three axis (9 entries) for each entry
  - Input pin capacitance must be characterized
  - DFF must be characterized for setup/hold, and all delays.
- Functional VHDL and Verilog models with unit delays must be provided
- Must demonstrate that a synthesized gate-level netlist produces same simulation results as RTL

Requirements for Layout

- Can use any technology that you wish, including demo technologies supplied with Cadence
  - Suggest use HP 0.5 since that is what we have technology files for here at MSU
  - See www.erc.msstate.edu/~pavan, see LAB #3.
- Detailed layout must be provided for all standard cells in chosen technologies
- 'Abstract' layout only required for IO cells
- Must demonstrate both
  - standard cell block (no IO cells)
  - Complete chip layout (IO cells + standard cell block)