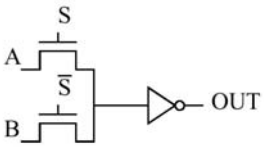
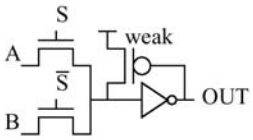
Prob #1

static power = Vdd * Iavg (clk = 0) = 2.5 * 325 ma = .81 W
dynamic power = Vdd*Iavg (clk=300 Mhz) – static power
= 2.5* 2.16A - .81 W = 4.6 W
Dynamic Cap = 4.6W/ (300 Mhz * 2.5V * 2.5V) = 2.45 nF

Prob #2

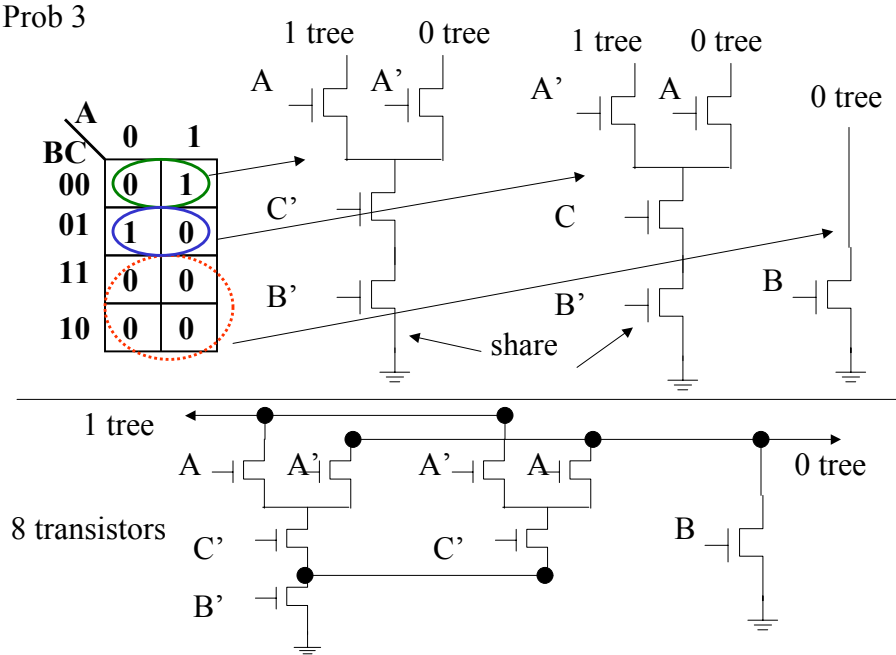


internal node at Vdd-Vt, static power dissipation problems because transistors not fully turned off. Especially bad at deep submicron.



Pulls up internal node to Vdd, but slower because pullup has to be overdriven.

Prob 3



Prob 4

Long channel fixed voltage delay scaling = $1/S^2$

Short channel fixed voltage delay scaling = $1/S$

In short channel devices, a combination of velocity saturation and mobility degradation (see Figure 2.28, page 53 of textbook) limits performance increases in deep submicron.

Prob 5

$K = (100 - 70) / (3 - 1) = 30/2 = 15$

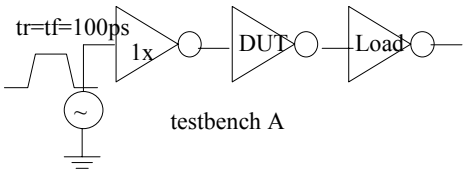
delay = noload + k * L

$15 = (70 - \text{noload}) / (1 - 0)$; noload = $70 - 15 = 55$ ps
for L = 5, delay = $55 + 15*5 = 55 + 75 = 130$ ps.

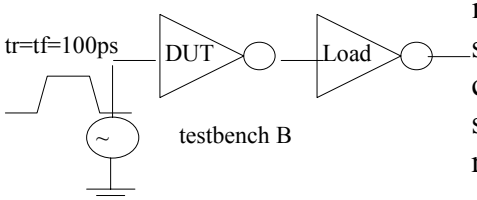
Prob 6

Only a single '1' to '0' transition is disallowed. All other transitions is valid (single 0 to 1, steady '0', steady '1')

Prob 7



DUT size will increase loading on 1X inverter, causing input slope to decrease, causing noload delay to INCREASE.



infinite drive strength of supply will keep input slope constant independent of DUT size, so no load delay will remain constant.

Prob 8

Use 3/1 inverter (high skew inverter) for domino logic inverter because this will optimize TPLH which is the only transistion that can occur during evaluation.

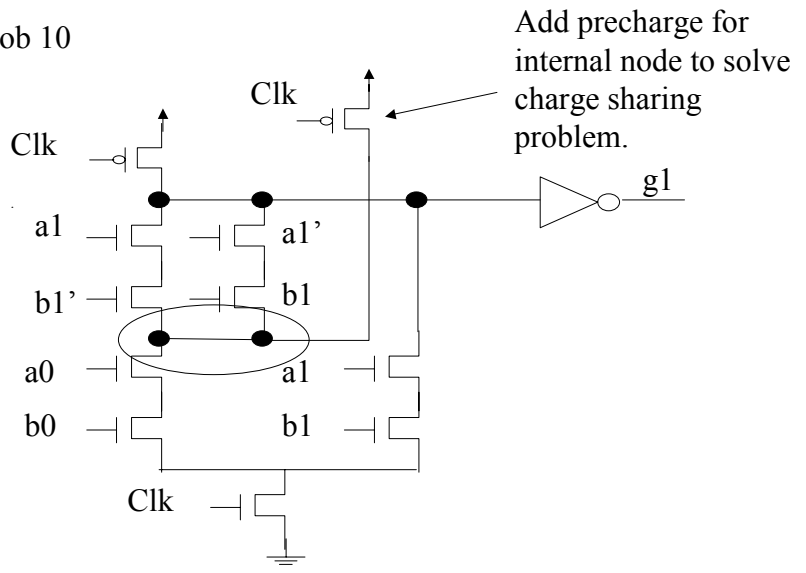
Use 1.4/1 inverter for low power since this will have the smallest capacitance value of the three inverters.

Prob 9

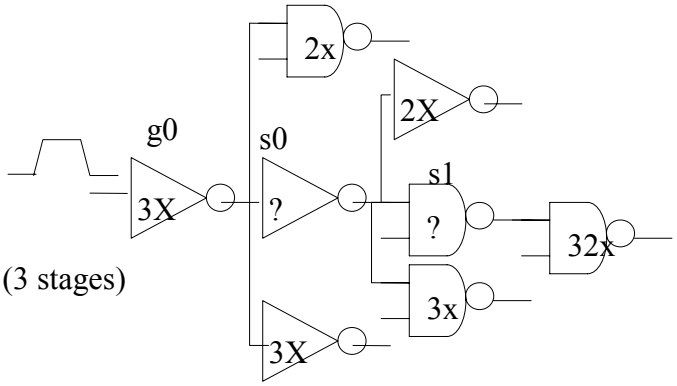
Use all 1X sizes for first step.

For second step, when driving gate becomes current gate, keep gate size found in the first iteration, so initial gate size of S0 will be 3X.

Prob 10



Prob 11



N = 3 (3 stages)

H = (32 * 4)/ (3 * 3) = 14.2

G = g_g0 * g_s0 * g_s1 = 1 * 1 * 1.3 = 1.3

B = 1 (ignore branching effort first iteration)

F = B * G * H = 18.4

optimum stage effort = $(F)^{1/3} = (18.4)^{1/3} = 2.64$

Prob 11 (cont)

S1 size = (beff_s1=1) * (g_s1=1.3) * (C_32x = 32*4) / Fopt
= 1 * 1.3 * 128 / 2.64 = 63

S0 size = (beff_s0=1) * (g_s0 = 1) * (C_s2 = 63) / Fopt
= 1 * 1 * 63 / 2.64 = 23.9

2nd iteration – compute branch efforts

beff_s1 = 1

beff_s0 = (2*3 + 3*4 + S1_size)/S1_size = (6+12+63)/63 = 1.3

beff_g0 = (2*4 + 3*3 + S0_size)/S0_size = (8 + 9 + 23.9)/23.9 = 1.7

B = beff_s1 * beff_s0 * beff_g0 = 1 * 1.3 * 1.7 = 2.2

F = B * G * H = 2.2 * 1.3 * 14.2 = 40.6

opt stage effort = $(40.6)^{1/3}$ = 3.4

S1 size = (beff_s1=1) * (g_s1=1.3) * (C_32x = 32*4) / Fopt
= 1 * 1.3 * 128 / 3.4 = 48.9

S0 size = (beff_s0=1.3) * (g_s0 = 1) * (C_s2 = 48.9) / Fopt
= 1.3 * 1 * 48.9 / 3.4 = 18.7

gate sizes S1 = 48.9/ 4 = 12.2 = 12 X

S0 = 18.7/3 = 6.2 = 6 X