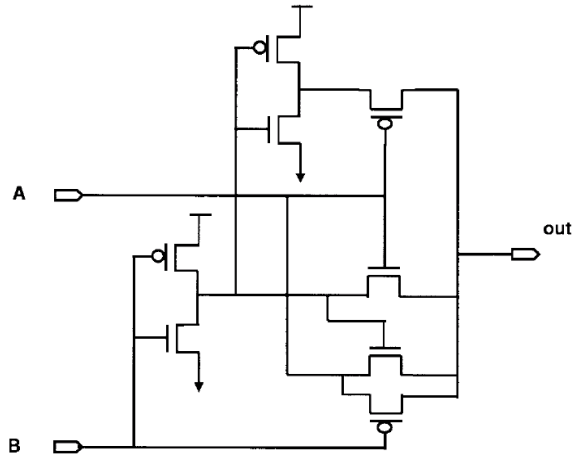
EE 8273 Test #1 Solutions - Fall '00 – Reese

Work all problems. Closed book, closed notes; You may use the supplied reference material.

1. (5 pts) Give the truth table of the gate below. What is the logic function?



XOR Function

2. 5 pts. A gate delay was measured as 3 ns in a 1.6u process. What would the expected gate delay be in a 1.2u process? *Use long channel scaling model, delay scales by $1/S^2$. S = 1.6/1.2 = 1.3*
*New delay = 3 ns /(1.3 * 1.3) = 1.7 ns*

3. 5 pts. A gate delay was measured as 300 ps in a 0.5u process. What would be the expected delay in a 0.25u process? *Use short channel scaling model, delay scales by 1/S. S = 0.5/0.25 = 2.*
New delay = 300 ps/2 = 150 ps.

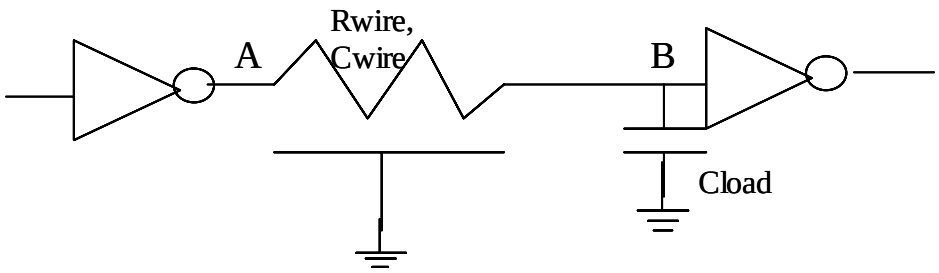
4. (6 pts) What is the difference in Resistance between a 1mm length wire in a 0.5u process and a 1.mm length wire in a 0.25u process?
   i) Assume the thickness of the metal wire is not scaled between 0.5u and 0.25u.
   S= 2, *L is constant, Thickness is constant, New W = Old W/2, so new R = 2 * Old R.*

   ii) Assume the thickness of the metal wire is scaled between 0.5u and 0.25u.
   S = 2, L is constant, Thickness scales up by 2, New = Old W/2, so New R = Old R.

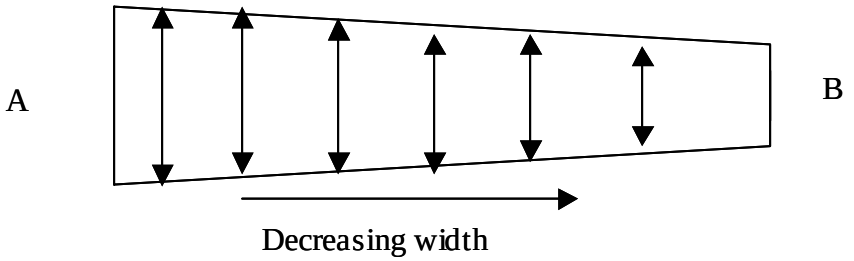
5. (5 pts) What is the Capacitance to substrate difference between 1 mm length wire in a 0.5u process and a 1 mm length wire in a 0.25u process?
   Cox scales down which increases Cap by S, but Width scales down by S which decreases Cap by S, so new Cap = old Cap.

6. (5 pts) Draw a circuit that you will use to measure the no-load delay of an inverter. I don't need any Spice, just explain your measurement setup (recall that no-load delay remains constant as transistor sizes are scaled upwards).
   Use a voltage source to drive the inverter which has no load. DO NOT use a 'driving' inverter to supply the input since the slope of the waveform supplied by the driving inverter will be affected by the different sizes of the inverter under test, giving incorrect no-load values.

7. (5 pts) In the circuit below, what conditions are needed for the delay from Point A to Point B to be significantly reduced if the width of the wire is doubled? *Cwire << Cload*



8. (5 pts) It has been shown that wire-tapering (see diagram below) of long wires can lead to reduced power dissipation in the wire without significantly impacting the wire delay from A to B. Why does this work?



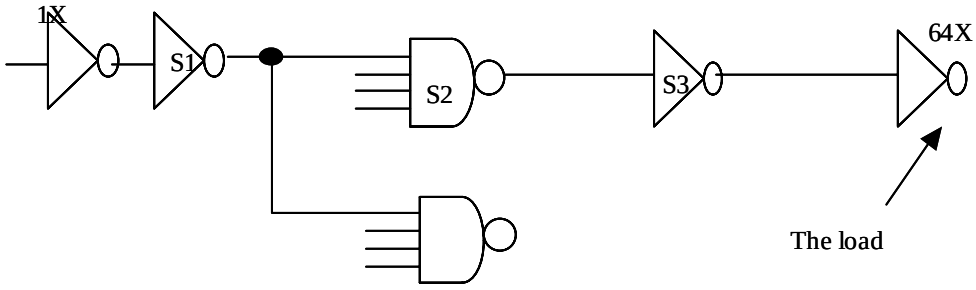
The Elmore delay equation says that the biggest contribution to the delay will be the R value near the source. So decreasing the width will affect the R values that are far away from the source ,which minimizes impact on delay. However, the decreasing width will reduce C wire, so power dissipation is decreased.

9. (6 pts) We did some characterizations that tried to come up with a capacitance value for a gate that could be used to estimate dynamic power dissipation for that gate. We found that this value scaled as expected when going from 1.6u to 0.5u, but did not scale as expected when going from 0.5u to 0.25u. Why did this happen? Explain the sources of dynamic power, and why the C value we measured/computed did not scale as expected.

   *Total Dynamic power is Cswitch*Vdd^2*F + short circuit (crowbar) current. Our power measurement measured Total Dynamic power, but we calculated 'C' as if the power all due to the switched capacitance and neglected the short circuit current. Short circuit current added more to our 'C' value as we scaled down at submicron technologies, which helped keep our 'C' constant.*

10. (6 pts) Explain how to measure/compute Tau, and Pinv for the logical effort model. Draw a circuit, show any computations/measurements that must be done. *SEE NOTES.*

11. Assume Pinv = 6, Pnand4 = 24, Tau = 8, g_inv = 1, g_nand4 = 2.



7 loads identical to S2

A. (10 pts) For the circuit above, compute the sizes for S1, S2, S3 for minimum delay using the logical effort approach.

N = 4. G = 1 * 1 * 2 * 1 = 2, H = 64/1, B = 1*8*1*1 = 8.
F min = $F^{1/4}$ = $(GBH)^{1/4}$ = $(2*8*64)^{1/4}$ = 5.7

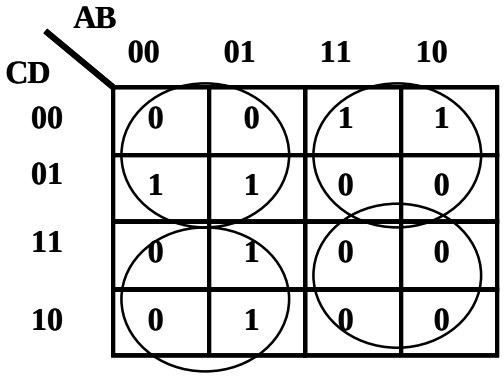
Cin(S3) = 64/Fmin = 11.3. Cin(S2) = 2*11/Fmin = 4
Cin(S1) = 8 * 4/Fmin = 5.7.

B. (4 pts) What is the absolute predicted minimum delay?
Min delay = tau (N * $F^{1/N}$ + Pinv + Pinv + Pnand4 + Pinv)
= 8 (4 * 5.7 + 3 (6) + 24) = 517

C. (4 pts) Assume the 1x inverter has PMOS = 4 * Lam, NMOS = 2*LAM (a 2/1 inverter). Based upon your calculated size for S2, give the PMOS, NMOS transistor sizes for your sized Nand4 gate.

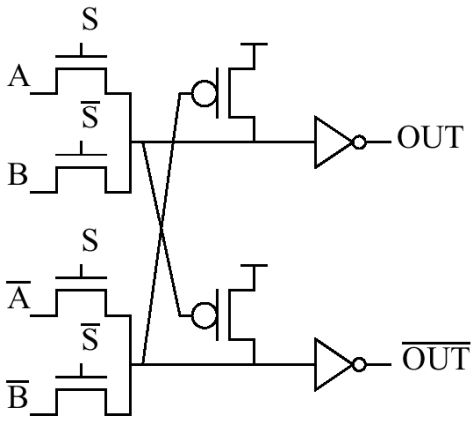
Size = 4X inv. So Nand4 (NMOS + PMOS)/ Inv (NMOS + PMOS) = 4
NAND4 (NMOS + PMOS) / (4 +2) = 4.
NAND4 is already typically sized as NMOS = 8, PMOS =4, so (4+8)/(4+2) = 12/6 = 2.
So, just double the size of the NAND4, NMOS = 16, PMOS = 8.

12. (8 pts)For the K-map below, give a DCVSL implementation that will maximize the transistor sharing.

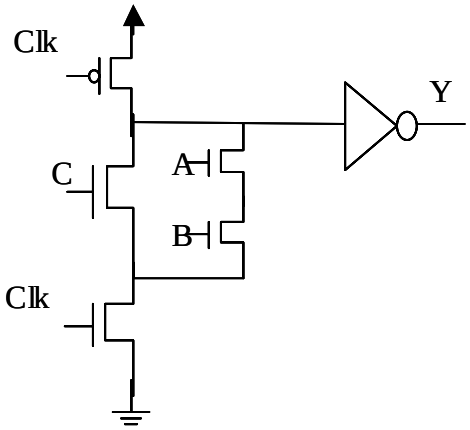


Work out solution from this, minimum sharing was 12 transistors.

13. (5 pts) Why is the cross coupling and PMOS-pullups included in the CPL gate below? What problem are they trying to solve? *Trying to solve power dissipation problem because input nodes to inverters will be one Vt below VDD. PMOS pull-ups pull these nodes all the way up to Vdd.*



14. (6 pts) Implement the equation F = AB +C as a domino logic gate.



15. (5 pts) What is a concern with domino logic and a slow clock frequency? How can you address this concern?

A slow clock frequency may allow the charge on the pre-charged N-Tree output to leak off before the evaluation period is over. A 'Weak' Keeper (a weak PMOS whose gate is tied to the output of the static inverter) can be used to hold the precharge value.

16. (5 pts) What is the constraint on input transitions to a domino logic gate?

During evaluation an input may:
Remain high
Remain low
Make single low to high transistion.