EE 8273 Test #1 - Fall '01 – Reese

Student ID: _____ (no names please)

Work all problems. Closed book, closed notes, open calculator. When asked for explanations, be concise.

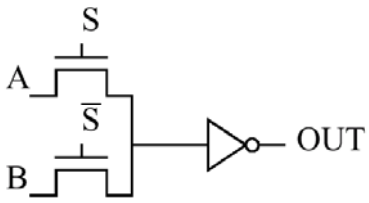
1. (10 pts) During the power characterization of a microprocessor the following measurements were made:
   average power supply current of 325 mA @ 2.5V when clock is stopped
   average power supply current of 2160 ma @ 2.5 V when clock frequency = 300 Mhz

   a. What is the static power consumption? (in W)?

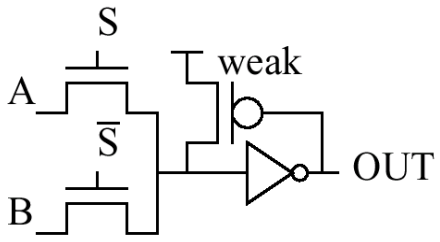
   b. What is the dynamic power consumption (in W)?

   c. What is the effective dynamic switched capacitance of this processor?

2. (10 pts) a. What was a concern in terms of speed and/or power for the mux implementation shown below?



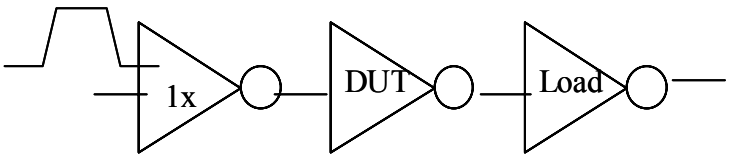
b. How did the mux implementation below address the concern in implementation (a)? What was the tradeoff (answer in terms of speed or power).



3. (10 pts) Implement the equation F (A,B,C) = AB'C' + A'B' C as a DCVSL gate. Use transistor sharing between the F and F' pulldown trees such that the total transistor count in the pulldown trees is 8 transistors or less.

4. (6 pts) For fixed voltage technology scaling, what is the delay scaling for long channel devices? For short channel devices? Why is there a difference between these?

5. (10 pts) For the test setup shown below, the following measurements were made:



TPLH (dut = 1x, Load = 1x) = 70 ps
TPLH (dut = 1x, Load = 3x) = 100 ps

a. For the simple RC delay model, what is the predicted noload delay?

b. For the simple RC delay model, what is the predicted delay for dut = 1x, Load = 5x ?

6. (8 pts)

For domino logic, which input transitions below are allowed? (circle either ALLOWED or DISALLOWED)

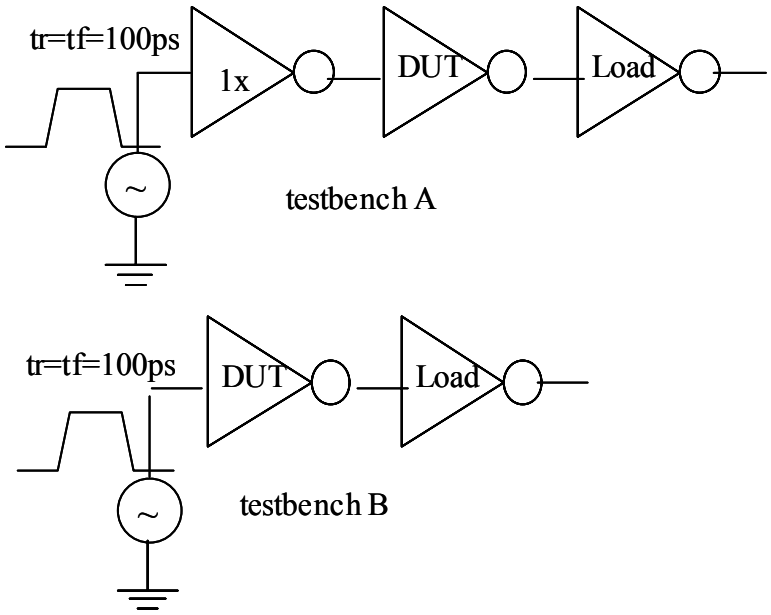
a. steady '0' throughout evaluation ALLOWED DISALLOWED

b. steady '1' throughout evaluation ALLOWED DISALLOWED

c. a single '1' to '0' transition during evaluation ALLOWED DISALLOWED

d. a single '0' to '1' transition during evaluation ALLOWED DISALLOWED

7. (10 pts) For the two testbenches shown below, answer the following questions:



Assuming that the DUT is varied between 1X and 6X, and LOAD is varied between no-load and 6X, what would you expect the NOLOAD delay measurements for DUTs 1X to 6X to do?

a. for Testbench A increase decrease remain relatively constant

b. for Testbench B increase decrease remain relatively constant

c. If you chose different answers for (a) and (b), explain why.

8. (8 pts) For Domino logic:

a. If you were optimizing for SPEED, the output inverter would be sized as:
3/1 2/1 1.4/1

Explain your answer.

a. If you were optimizing for POWER, the output inverter would be sized as:
3/1 2/1 1.4/1

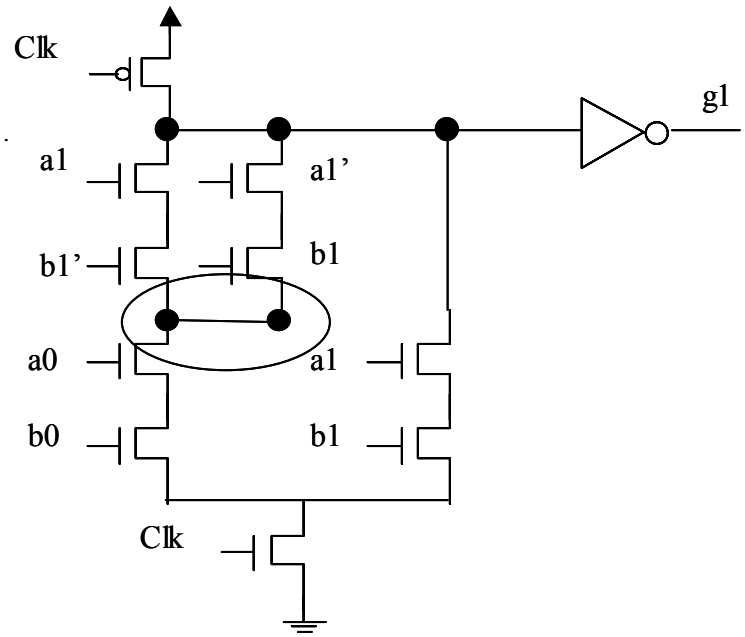
Explain your answer.

9. (8 pts) Refer to the circuit for problem #11. Assume the tilos algorithm is being used to size gates S0 and S1.

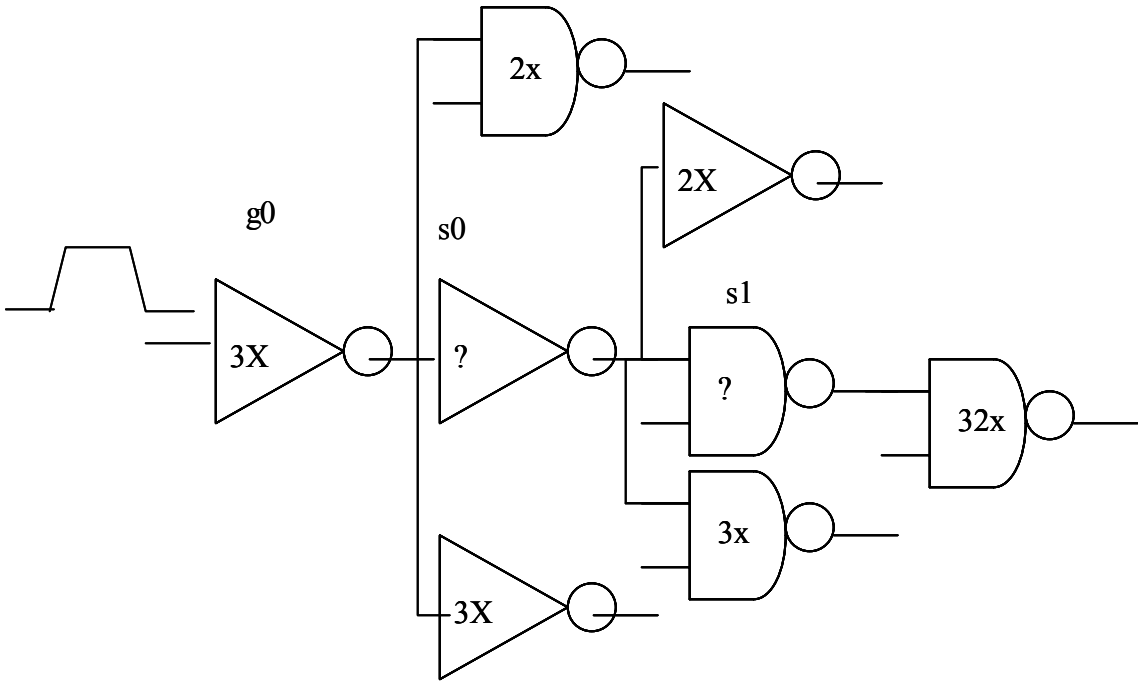
a. What are the initial sizes chosen for gates S0 and S1? (Assume we have sizes that range from 1x to 10x).

b. Assume that the Tilos algorithm chooses a size of 5X for gate S1 and 3X for S0 when current gate = S1 and driving Gate = S0. For the next stage of the algorithm, the current gate is set to S0, and the driving gate = G0. What is the initial size used for gate S0 in this stage of the algorithm?

10. (5 pts) The circled node below in the domino logic gate has a charge sharing problem. Show a modification to this circuit that would alleviate the charge sharing.



11. (15 pts) Use the Leffort approach to optimize the sizes of gates S0 and S1 below to minimize delay. Assume gnand = 1.3, inverters are sized as 2/1, nand2 sized as 2/2. Perform only TWO iterations of the algorithm. Answer the questions below from your calculations. All off path loads are FIXED. Assume there is no limit on gate sizes. Show all work if you expect to earn any partial credit.



a. First iteration optimum stage effort _____

b. Second iteration optimum stage effort: _____

c. Gate size of S1 after 2nd iteration: _____

d. Gate size of S2 after 2nd iteration: _____