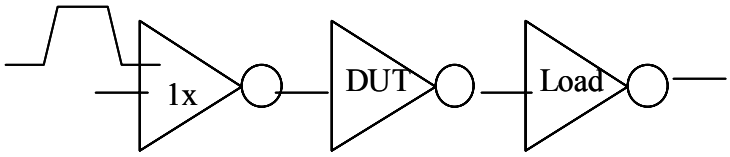
EE 8273 Test #1 Solutions Fall '02 – Reese

Work all problems. Closed book, closed notes, open calculator. When asked for explanations, be concise.

1. (5pts) Assume the test setup shown below. For the simple RC timing model of (Delay=Tnoload + Kcload), what is the minimum number Spice measurements would you need to characterize TPLH, TPHL for the DUT?
   Two spice measurements each for TPLH, TPHL (total = 4). One no-load measurement, one



   measurement at a typical LOAD value.

2. (5 pts)What is the principle accuracy problem with using the simple RC timing model?

   Measured Tnoload, 'K' value only good for the particular input slope used – the input transition time affects delay.

3. (6 pts) For an inverter, give the tables required for TPLH, TPHL for the 2D characterization method that we used in the first simulation. Give the number of tables required, and the axis for each table.

   Axis for each table: Input Transition time, Output Load
   Four Tables: TPLH, TPHL, Output transition time rising, Output transition time falling

4. (4 pts) As device sizes have shrunk, has CMOS static power dissipation become more or less of a concern? Explain why.

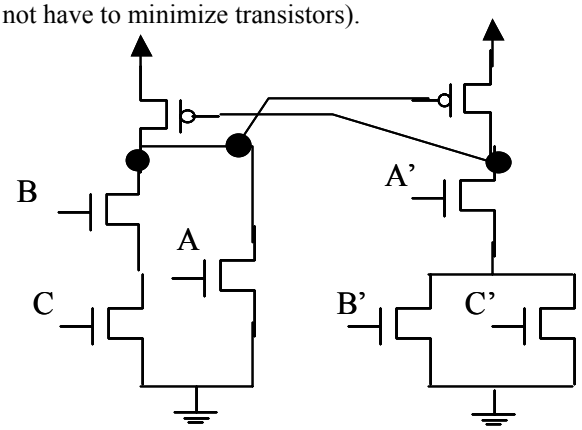
   Subthreshold current has increased – ie., transistors have become harder to turn off.

5. (4 pts) Give two sources of dynamic power dissipation in a CMOS circuit. Give an equation for the one that is of most concern.

   Capacitive Switching (P = C * Vdd *Vdd * f)

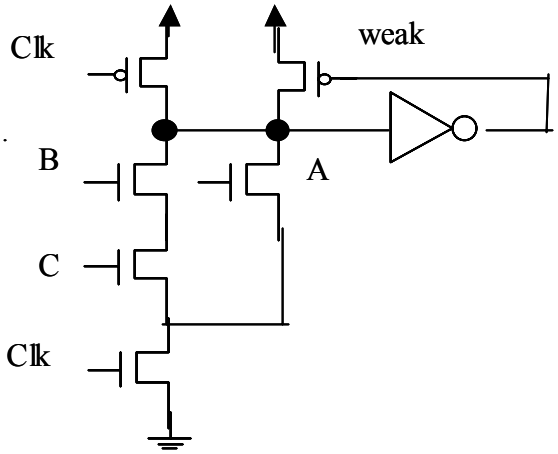
   Crowbar current – the short circuit current between Vdd and GND when a gate switches

6. (6 pts) Draw the DCVSL gate for the equation A + BC (you do not have to minimize transistors). What is the attraction of DCVSL?

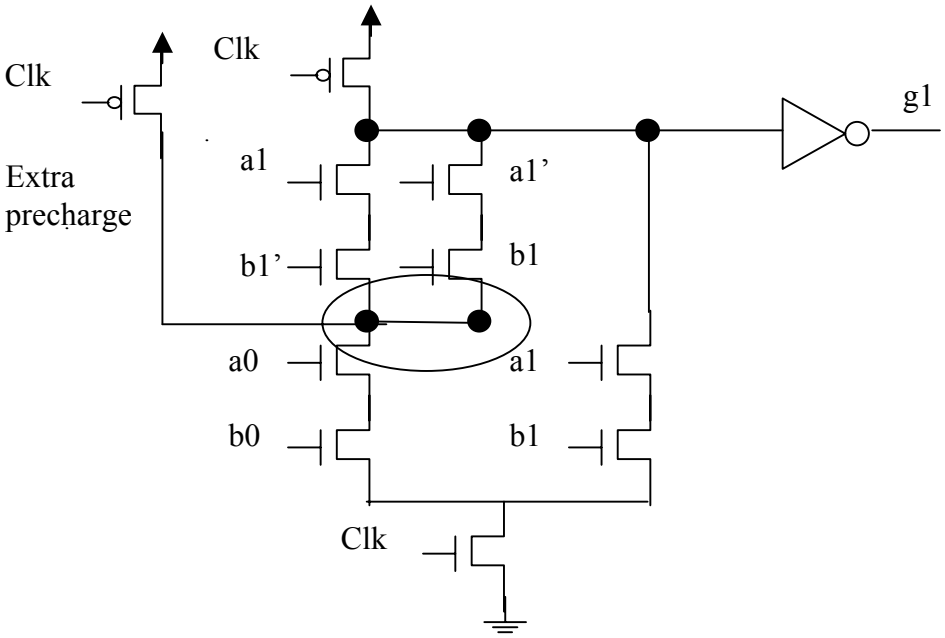


7. (6 pts) Draw the Domino gate for the equation A + BC.

8. (5 pts) Modify the gate diagram for the Domino gate above so that if the clock is stopped during evaluation, the gate output is kept stable.



9. (4 pts) Give an example of charge sharing in a domino gate and a method for fixing it.



10. (4 pts) What is charge coupling in a CMOS circuit? Give two examples.
A signal transition on one node causes a change in voltage on another node when there is no direct connection. Two examples: charge coupling between wires because of sidewall capacitance or layer-to-layer capacitance; coupling between source/drain and a floating gate.

11. (4 pts) Some circuits are classified as 'truly dynamic', i.e., they have 'dynamic nodes'. What does this mean?
There is a time period within the circuit whenever the node is not actively driven.

12. (4 pts) In a domino logic gate, which delay do I want optimized, TPLH or TPHL? Explain why.

Want to optimize the low to high transition on output of inverter, so TPLH.

13. (5 pts) In the Tilos algorithm, there is a 'driving' gate and a 'current' gate (the gate on the output of the driving gate). Explain the general algorithm loop involving these two gates. How were the sizes of these gates chosen?

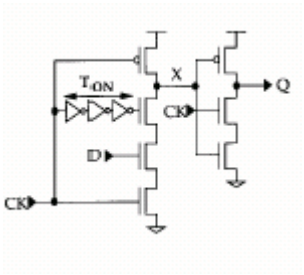
See notes.

14. (4 pts) Why is negative setup time a nice to feature to have in pipeline latches? |||

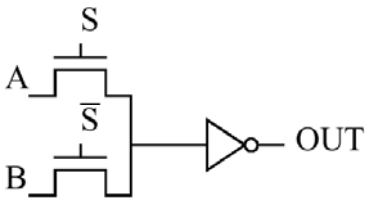
So that clock borrowing can be done – the input can change after active clock edge – this uses some of the evaluation time in the next pipeline stage – logic in pipeline stages do not have to be perfectly balanced.

15. (4 pts) All of the pulsed DFFs, pulsed latches we looked at had a common, distinguishing characteristic involving the clock – show this characteristic.

A delayed version of the clock is generated in the circuit via a string of inverters.



16. (3 pts) What was a concern in terms of power for the mux implementation shown below?



The node at the front of the inverter will have a threshold drop, so the PMOS in the inverter will not be fully turned off, causing more leakage current.

17. (3 pts) If a domino gate input goes from 0 to 1 during evaluation, can it make any other transition during evaluation? Why or Why not?

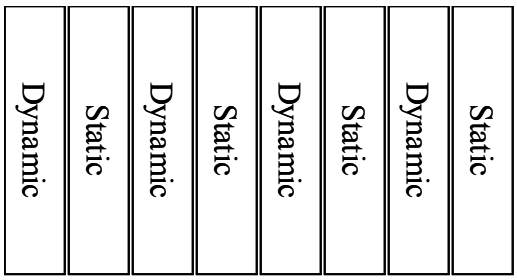
If the intended data value is '1', can make a transition back to '0' after the input value has been consumed by the destination gate.

18. (3 pts) If a domino gate input is initially a '1' at the start of evaluation, can it make any other transition during evaluation? Why or Why?

If the intended data value is '1', then a transition to '0' cannot be made because the '1' may have already been consumed and created a path to ground in the domino gate, setting the precharged node to zero.

19. (10 pts) Assume I have four stages of domino logic as shown below. The TPHL/TPLH of each dynamic stage is 100 ps/25 ps. The TPHL/TPLH of each static stage is 30/40 ps.

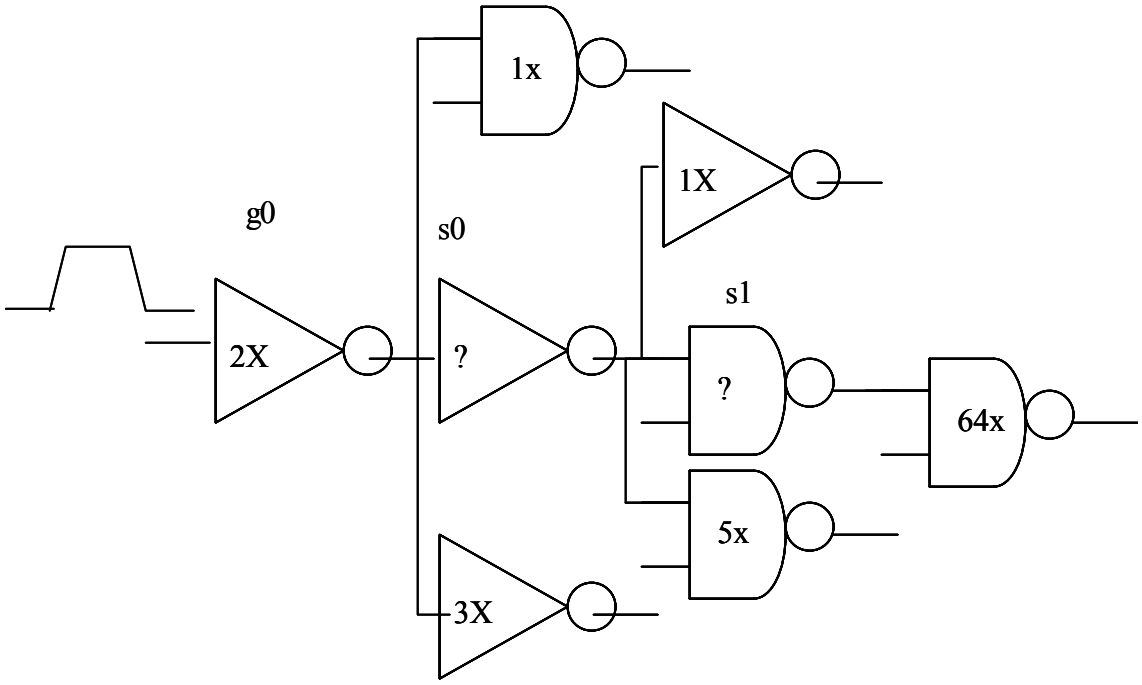
What is the maximum evalution time for this block of logic? (show work for partial credit)
What is the maximum precharge time for this block of logic (show work for partial credit).



Evaluation time for one gate:
TPHL (dynamic) + TPLH (static) = 100+40 = 140
Evaluation occurs in series, so 4 * 140 = 560 ps

Precharge time for one gate
TPLH (dynamic)+ TPHL (static) = 25 + 30 = 55 ps.
Precharge occurs in parallel, so 55 ps.

20. (13 pts) Use the Leffort approach to optimize the sizes of gates S0 and S1 below to minimize delay. Assume gnand = 1.3, inverters are sized as 2/1, nand2 sized as 2/2. Perform only TWO iterations of the algorithm. Answer the questions below from your calculations. All off path loads are FIXED. Assume there is no limit on gate sizes. Show all work if you expect to earn any partial credit.



1st iteration:
H = (64 * 4) / (2 3) = 42.67 ('64*4' because load has to be converted to transistor Width units).
G = 1 * 1 * 1.3 = 1.3
B = 1 (branching effort ignored)

F = G*B *H = 55.47; Optimum stage effort = $(55.47)^{1/3}$ = **3.81.**

Cin(s1) = ((64 *4) * 1.3* 1)/ 3.81 = 87.35. S1 size = 87.35/4 = **22X**
Cin(s0) = (87.35 * 1 * 1) / 3.81 = 22.93 S0 size = 22.93/3 = **7X**
Cin(g0) = (22.93 * 1 * 1) / 3.81 = 6.01 G0 size = 6.01 / 3 = **2X** (Check Works)

2nd iteration:

B = bs1 * bs0 * bg0

bs1 = 1
bs0 = ((1*3) + (5*4) + 87.35)/ 87.35 = 1.26
bg0 = ((1*4) + (3*3) + 22.93)/ 22.93 = 1.57

B = 1 * 1.26 * 1.57 = 1.98

F = 1.3 * 1.98 * 42.67 = 109.83 Optimum stage effort = $(109.83)^{1/3}$ = **4.79.**
Cin(s1) = ((64 *4) * 1.3 * 1)/ 4.79 = 69.48 S1 size = 69.48/4 = **17.5X**
Cin(s0) = (69.48 * 1 * 1.26) / 4.79 = 18.28 S0 size = 18.28/3 = **6X**
Cin(g0) = (18.28 * 1 * 1.57)/ 4.79 = 5.99 G0 size = 5.99/3 = **2X** (CHECK WORKS)