FPGA Advantage for HDL Design

The FPGA Advantage design flow provides the most effective HDL environment for designing FPGAs.

Major product features:

- A robust, HDL-based methodology for FPGA design
- Integrates HDL Designer Series™ for design creation and management, ModelSim® for simulation, and LeonardoSpectrum™ for synthesis
- One user interface drives the entire design process, offering push-button ease as well as power features for added control
- Iteration loops are decreased by seamlessly blending edit, compile, simulate, and synthesize steps
- IP and legacy HDL designs are easily incorporated, displaying hierarchy and optional graphical descriptions, enhancing design comprehension and reuse

A Single-Package Solution for FPGA Design

FPGA Advantage® provides an integrated HDL flow for designing FPGAs. FPGA Advantage enables design creation, simulation, and synthesis as operations flowing smoothly from one design step to the next. Quality of results and productivity are enhanced with the deep tool integration of design creation, simulation, synthesis, and debugging, surrounded by design management.

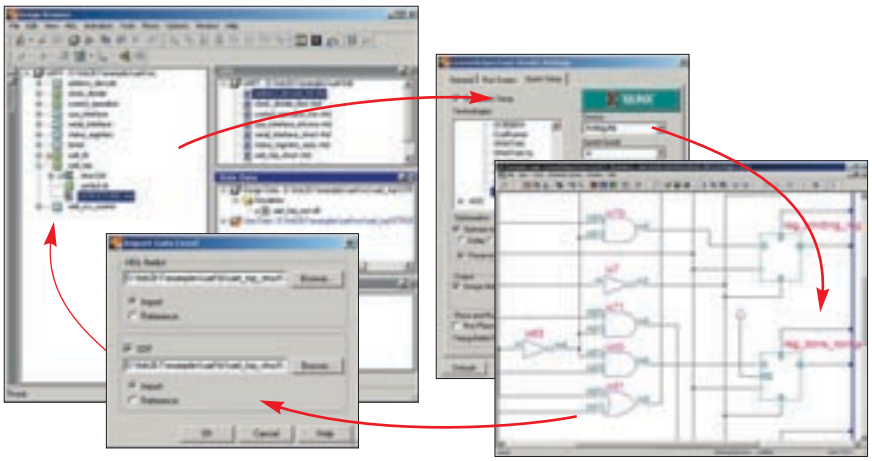
HDL Designer Series serves as the cockpit for design creation, reuse, and management, and is the invocation bridge to HDL simulation with ModelSim, and HDL synthesis with LeonardoSpectrum.

Each component of FPGA Advantage is a proven point tool, but the power comes from integrating these tools tightly together to create a unique HDL design methodology environment for VHDL and Verilog, on Windows® and UNIX®, for any design budget.

Design Creation

Design creation is a personal choice, and FPGA Advantage provides multiple design editors that accommodate both text and graphical preferences. The FPGA Advantage text editors include the Block Diagram editor for design partitioning and organization, Tabular I/O for rapid block signal definition, and the Interface-Based Design™ (IBD™) editor for defining the interconnection of components throughout the design hierarchy. FPGA Advantage's State Machine, Flow Chart, Truth Table, and Block Diagram editors speed design creation and automatically generate efficient VHDL and Verilog code. These text and graphical editors help both novice and experienced designers effectively manage increasing design complexity.

Understanding the need to reuse legacy designs and incorporate intellectual property, FPGA Advantage smooths the access to FPGA vendor IP and accepts VHDL and Verilog



FPGA Advantage creates a complete design cycle from entry to post place-and-route verification, with an easy push button flow. (All major FPGA vendors supported.)

source code designs. The hierarchy of these imported designs is immediately displayed and graphical representations can be optionally generated to accelerate the understanding of the imported code.

Design Documentation

FPGA Advantage supports OLE, postscript, and HTML export for documentation needs, making documentation easier and encouraging it throughout all the design development phases.

Simulation

Flowing from the FPGA Advantage Design Browser cockpit, design creation and simulation have a common interface that lets you automatically generate, compile, and invoke the design for simulation. With the enhanced debugging environment in FPGA Advantage, you can visualize the flow of logic through animated simulation with color changes, cross-referencing, and cross-highlighting between HDL source code and the corresponding graphical object. You can step incrementally through the HDL code and graphical objects, and view simulation probes on graphical objects to speed debugging. Viewing simulation in this manner, together with the simulation waveform comparison capability, enables quick and easy detection of bugs and rapid design iterations.

Synthesis

FPGA Advantage incorporates the most powerful FPGA synthesis solution available. The Design Browser automatically loads your design into the synthesis environment, ready for you to specify design goals and run optimizations. FPGA vendor tool integration and TimeCloser™ technology ensure that you quickly meet your design constraints. FPGA Advantage uniquely offers built-in design partitioning between multiple vendors and silicon technologies. With technology re-targeting, you can target FPGAs for prototyping ASICs, enabling low-cost production.

PRODUCT CONFIGURATIONS

	Language Support	Design Editors	Application	Licensing	Platforms	Software Tools Included
FPGA Advantage for Personal HDL Design	VHDL, Verilog, or mixed-HDL	Text, Graphics, or Pro (both Text and Graphics)	FPGA with ASIC option for Level 3	Nodelocked or Floating	Windows: 98, NT, 2000, XP	HDL Author, ModelSim PE, LeonardoSpectrum (Level 2 or 3)
FPGA Advantage with Personal Simulation	VHDL, Verilog, mixed-HDL	Text, Graphics, or Pro (both Text and Graphics)	FPGA with ASIC option for Level 3	Nodelocked or Floating	Windows: 98, NT, 2000, XP	HDL Designer, ModelSim PE, LeonardoSpectrum (Level 2 or 3)
FPGA Advantage for HDL Design	VHDL, Verilog, HDL, mixed-HDL, or PLUS (separate VHDL and Verilog licenses)	Text, Graphics, or Pro (both Text and Graphics)	FPGA with ASIC option for Level 3	Floating	Windows: 98, NT, 2000, XP UNIX: Sun Solaris 7, 8; HP-UX 11.0	HDL Designer, ModelSim SE, LeonardoSpectrum Level 3, LeonardoInsight

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