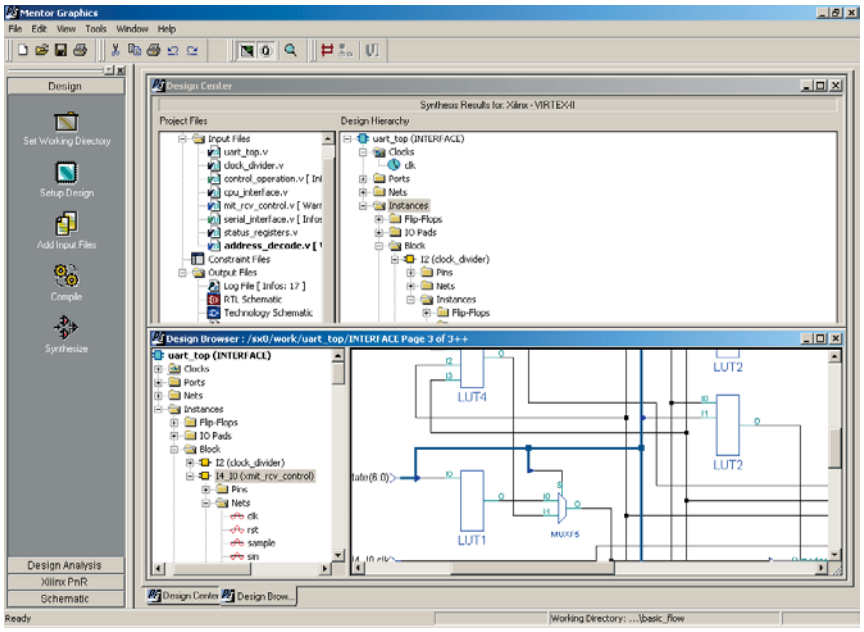
Precision Synthesis

D A T A S H E E T



The intuitive Precision Synthesis graphical user interface minimizes the learning curve while maximizing productivity.

Major product features:

- Design Bar guides you step-by-step through synthesis, analysis, and place-and-route
- Integration of the industry's most popular place-and-route tools provides easy access to back-end implementation and analysis tools
- Language neutrality supports any combination of VHDL, Verilog, and EDIF
- Built-in schematic viewing of your RTL and FPGA design
- Register retiming moves registers across logic to improve performance
- Interactive PreciseTime quickly performs *what-if* timing analysis
- Constraint analysis identifies missing constraints

Intuitive Synthesis for Today's FPGA Designs

As FPGAs continue to grow in size and complexity, designers need a synthesis tool they can depend on. Time-to-market pressures leave little time to become tool experts; yet performance requirements demand excellent results. Precision™ Synthesis delivers on this promise. A highly intuitive interface drives advanced FPGA synthesis technology to deliver correct results without iterations. Timing constraints, coupled with state-of-the-art timing analysis, guide optimization when and where it's needed most, achieving excellent results for even the most aggressive designs. But power doesn't need to come at a price. Novices will quickly feel like experts using an interface that guides them step-by-step through the synthesis process. Whether you design one FPGA per month or one FPGA per year, Precision Synthesis will keep you on schedule.

ASE Optimization

A suite of unique algorithms, called Architecture Signature Extraction (ASE) optimization automatically focuses specific optimizations on areas of the design most likely to hinder overall performance, such as finite state machines, cross-hierarchical paths, and paths with excessive combinational logic. ASE uses an automated, heuristic approach to deliver smaller, faster designs without iterative, manual intervention.

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PreciseTime Timing Analysis

PreciseTime timing analysis locates the true critical paths in even the most complicated designs and clocking schemes. A combination of timing analysis technologies are used to correctly handle even the most complex circuits, eliminating workarounds and hand timing verification, while increasing confidence in the results.

ASE Optimization

With Precision Synthesis, it's knowledge of the design that's important, not knowledge of synthesis tool settings, options, or attributes. Timing constraints, based on the industry standard Synopsys Design Constraint (SDC) format, are all that's needed to deliver correct results, without iterations. You spend time designing, not synthesizing.

Optimization Without Boundaries

Advanced optimization technology breaks down performance-limiting design barriers, such as register, hierarchy, and operator boundaries. A powerful retiming algorithm balances logic across register boundaries; hierarchy optimization minimizes logic between modules; and pipelining moves registers into multipliers. Precision Synthesis identifies when and where to employ these algorithms, which can improve circuit performance by up to 70 percent.

FSM Optimization

Finite state machines (FSM) are automatically detected and optimized. Complete analysis is performed on each FSM to locate and eliminate all unnecessary states. A variety of encoding styles are then evaluated to determine the best implementation for your design and target technology.

PreciseTime Analysis

A designer's skill and experience is fully utilized with visibility into the implementation of an RTL design. Precision Synthesis provides a built-in set of powerful analysis features that give you the information necessary to make important tradeoffs.

Interactive Timing Analysis

The information you receive about device timing should not be limited to a few pre-selected paths in a synthesis report. Interactive timing analysis quickly generates detailed timing reports from any port, pin, or instance in the design. Timing queries can be initiated throughout the user interface, including selected objects in the schematic viewer.

Constraint Analysis

Missing timing constraints result in incomplete timing analysis and may allow timing errors to go undetected until board debug. Precision Synthesis eliminates this unnecessary schedule risk by performing a complete constraint analysis prior to synthesis, ensuring that designs are fully and accurately constrained. First time success on your printed circuit board requires a fully and accurately constrained design during synthesis.

Schematic Viewing with Critical Path Fragment Filtering

An integrated schematic viewer provides a clear visualization of the synthesis process. High-level RTL schematics help you determine the impact of coding styles, while detailed technology schematics show where and how device-specific resources (such as RAM and ROM) are utilized. Patented path viewing and filtering technology displays concise fragments of timing critical logic.

Visit our web site at www.mentor.com/synthesis/precision for the latest product news.

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Printed on Recycled Paper

5-02-WCI 1020430