Transitioning to Precision RTL Synthesis

Precision RTL Synthesis Overview

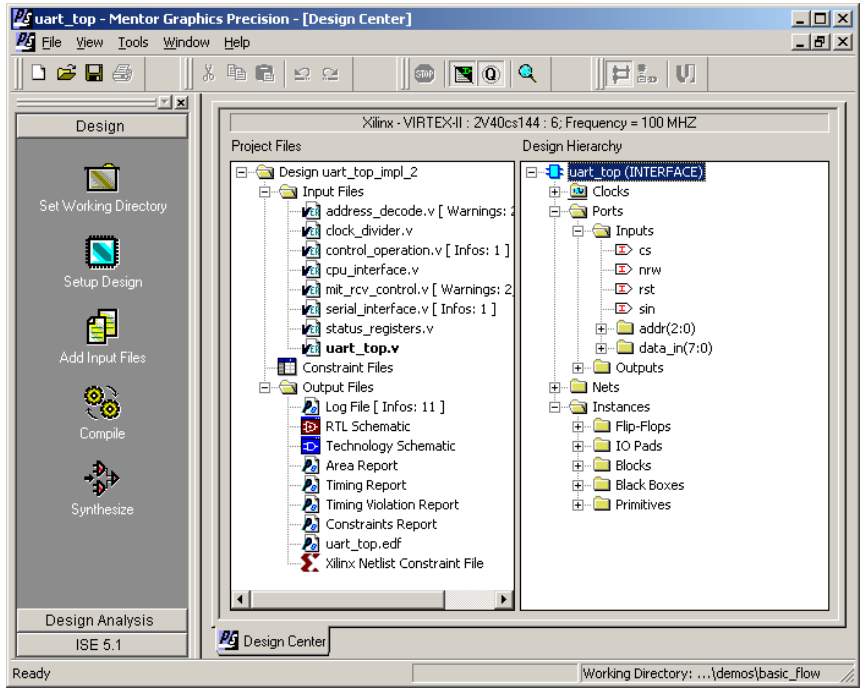
What is Precision Synthesis?

- **Precision is a synthesis technology platform from which 3 FPGA synthesis products have been introduced. These products include**
  - **Precision RTL**
    - **Intuitive FPGA synthesis providing excellent results and advanced design analysis capabilities**
  - **Precision Physical**
    - **Performance oriented FPGA synthesis employing placement based physical optimization techniques**
  - **Precision C**
    - **Algorithmic C and C++ synthesis which uses high-level synthesis techniques targeting DSP applications**
- **All products share a common user interface**

The Precision User Interface

- **Precision Synthesis provides a highly productive FPGA synthesis environment**
- **Easy to learn:**
  - **Intuitive interface drives the synthesis process**
  - **Dedicated to the task of FPGA synthesis**
- **Quick results:**
  - **FPGA optimizations have been automated to provide excellent results the first time**

The Precision Design Center



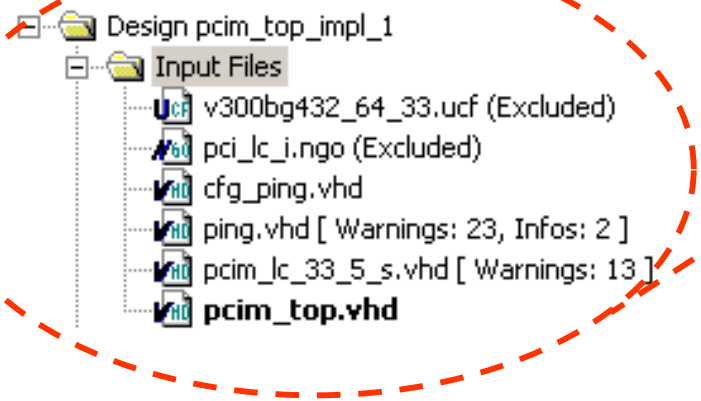
Supports SDC for timing constraints

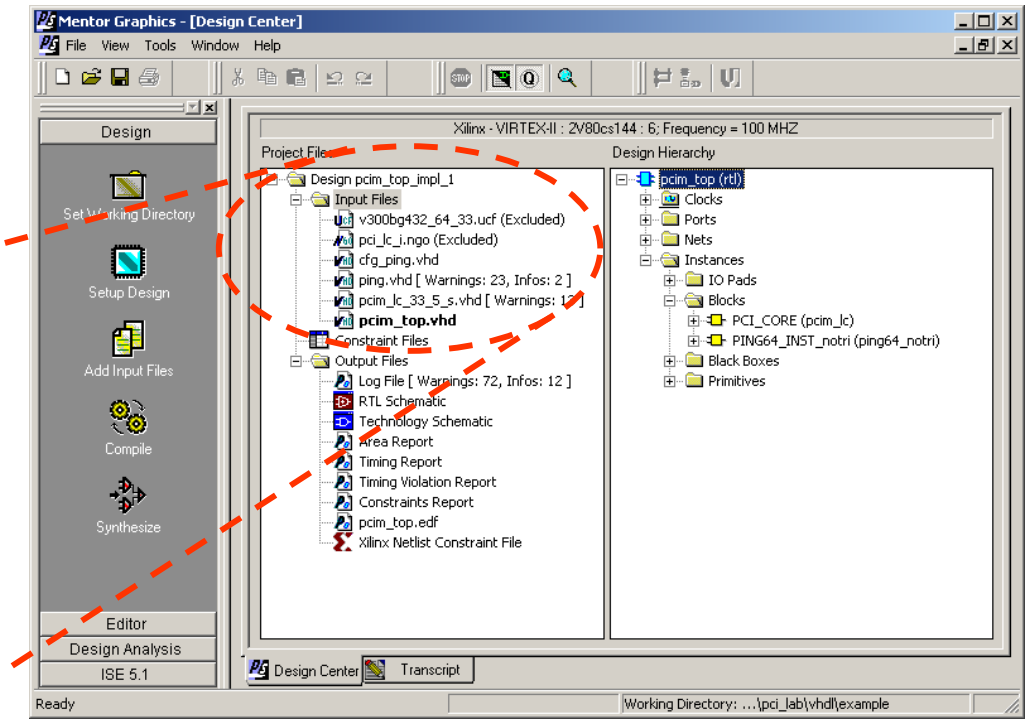
- **Industry expertise is leveraged through the support of Synopsys Design Constraints (SDC) for specifying timing in a design**
- **Supports full SDC including get and find commands**

```
# Clock Constraints
create_clock clk -period 10

# Input Constraints
set_input_delay 2 data_en -clock clk
set_input_delay 3 data_in* -clock clk

# Output Constraints
set_output_delay 3 data_stb -clock clk
set_output_delay 8 data_out* -clock clk
```

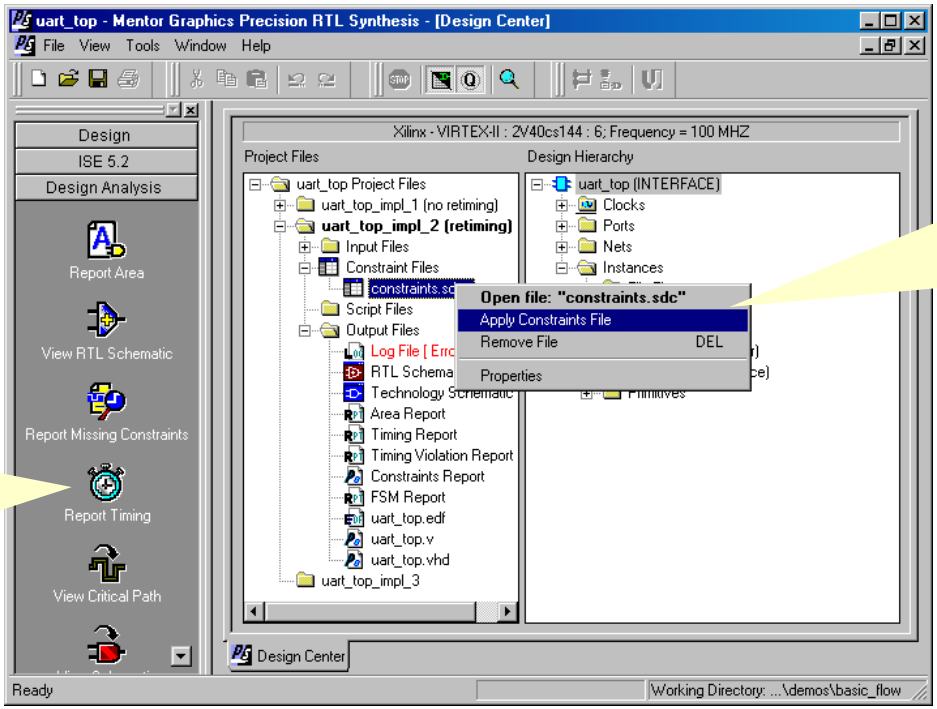
Includes “Built-in” Design Flows

- Common FPGA design flows have been “built-in” to Precision to provide “push-button” automation
- Flows include
  - Xilinx PCI Core
  - Altera LogicLock
  - Place and Route





Includes fully interactive static timing analysis

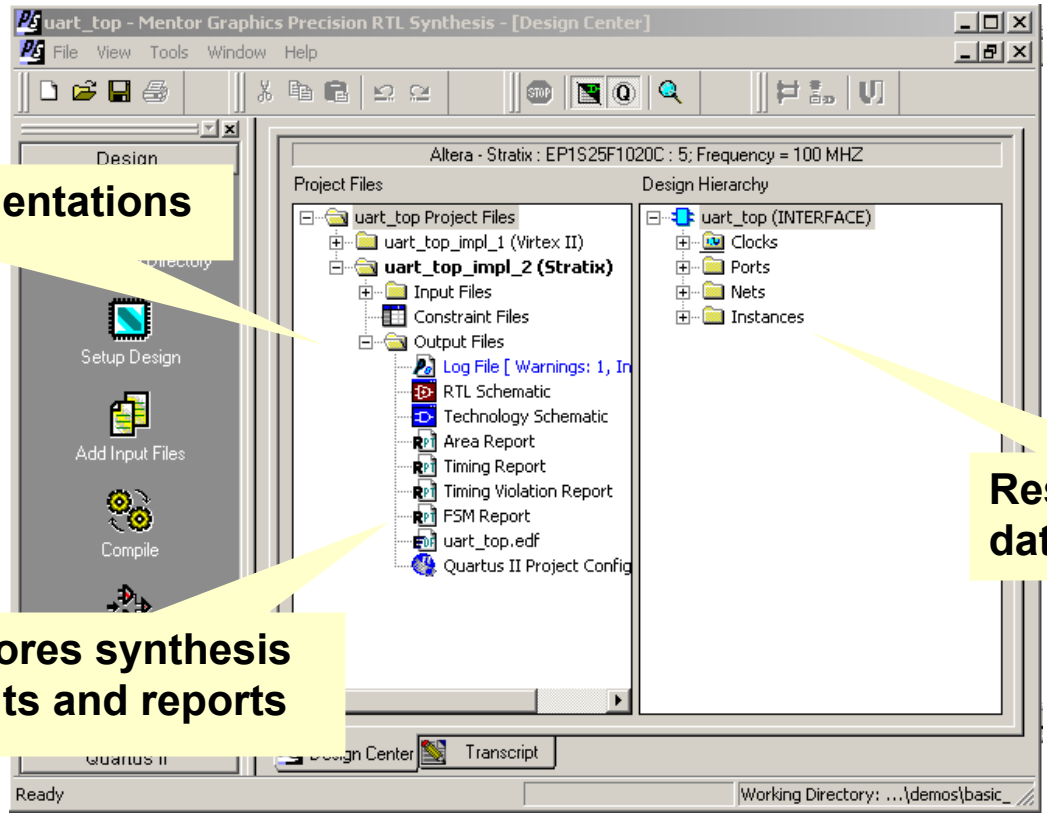


Constraints can be modified and reapplied to a synthesized database.

Once “applied” an incremental timing analysis can be performed

- **Incremental timing analysis allows rapid constraint debug iterations**
- **Nodal timing analysis technology rapidly recalculates timing information**

Provides true project management



multiple implementations

Restores synthesis results and reports

Restores design database

- **Key Benefits**
  - Restores previous optimization results for analysis
  - Easily switch between multiple revisions

Fully Integrated into FPGA Advantage®

- Complete FPGA design flow including
  - HDL Designer Series™
  - ModelSim®
  - Precision Synthesis
- Delivers FPGA
  - Project management
  - Design creation and reuse
  - Enhanced simulation and synthesis analysis
  - Linkage to FPGA vendor P&R
  - Post P&R gate level verification
  - Design documentation vehicles

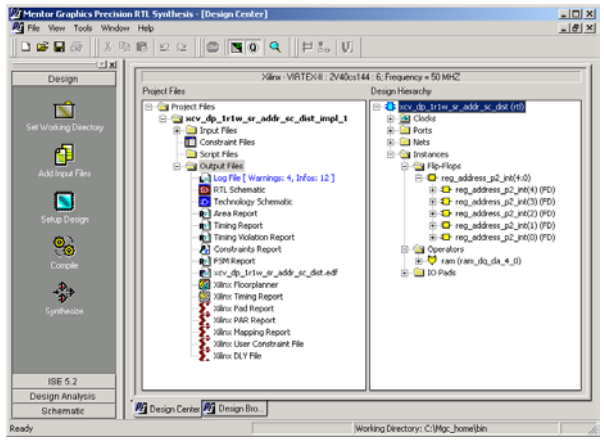
This transition program is for LeonardoSpectrum Level 3 customers only. FPGA Advantage customers will be offered a transition in the near future.

Differences between Precision RTL Synthesis and LeonardoSpectrum

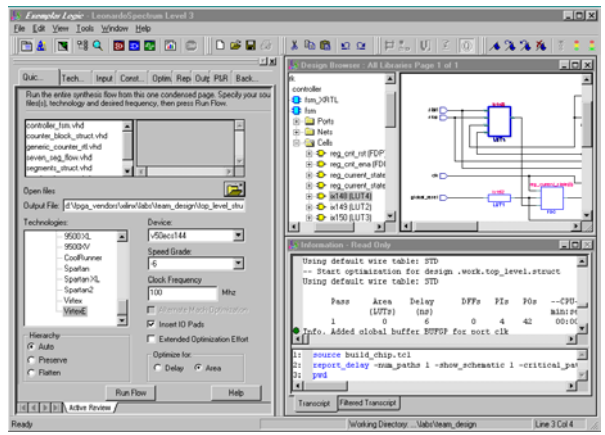
Improved usability for new users

- Precision employs a single interface, called the “Design Center” to drive the synthesis process
  - Optimizations are automated
  - Many unnecessary settings were eliminated
- LeonardoSpectrum uses a tab based interface to present an extensive set of options to the user
  - Considered intimidating by new users

Precision



LeonardoSpectrum



Timing Closure achieved with fewer iterations

- **Precision automatically configures optimization based on timing constraints**
- **LeonardoSpectrum requires optimization to be configured through user defined command settings**

Precision Timing Report

```
Critical path #1, (path slack = 0.59):

SOURCE CLOCK: name: CLK period: 10.000000
     Times are relative to the 1st rising edge
  DEST CLOCK: name: CLK period: 10.000000
     Times are relative to the 1st falling edge

NAME                                          GATE       DELAY    ARRIVAL DIR
pci0_dec0_modgen_counter_PCNT_reg_q(7)/C      FDCPE                   0.00   up
pci0_dec0_modgen_counter_PCNT_reg_q(7)/Q      FDCPE      0.71         0.71   up
pci0_dec0_modgen_eq_92_ix22/I0                LUT4_L                  0.71   up
pci0_dec0_modgen_eq_92_ix22/LO                LUT4_L     0.33         1.04   up
pci0_dec0_modgen_eq_92_ix23/S                 MUXCY_L                 1.04   up
pci0_dec0_modgen_eq_92_ix23/LO                MUXCY_L    0.37         1.40   up
pci0_dec0_modgen_eq_92_ix27/CI                MUXCY_L                 1.40   up
pci0_dec0_modgen_eq_92_ix27/LO                MUXCY_L    0.04         1.44   up
pci0_dec0_modgen_eq_92_ix31/CI                MUXCY_L                 1.44   up
pci0_dec0_modgen_eq_92_ix31/LO                MUXCY_L    0.04         1.48   up
pci0_dec0_modgen_eq_92_ix35/CI                MUXCY                   1.48   up
pci0_dec0_modgen_eq_92_ix35/O                 MUXCY      1.09         2.58   up
io0_ix1299/I0                                 LUT4                    2.58   up
io0_ix1299/O                                  LUT4       0.61         3.19   up
io0_ix1370/I0                                 LUT4                    3.19   up
io0_ix1370/O                                  LUT4       0.47         3.66   up
io0_ix1197/I3                                 LUT4                    3.66   up
io0_ix1197/O                                  LUT4       0.47         4.13   up
io0_reg_RAM_2CSn/D                            FDP_1                   4.13   up

                Initial edge separation:          5.00
                Source clock delay:       -       1.18
                Dest clock delay:         +       1.18
                                          ------------
                Edge separation:                  5.00
                Setup constraint:         -       0.28
                                          ------------
                Data required time:               4.72
                Data arrival time:        -       4.13
                                          ------------
                Slack:                            0.59
```

Positive Slack indicates timing has been met

Improved Optimization Technology

- **Precision includes the following new optimization technology for improving chip performance**

Algorithm	Benefit
Advanced FSM	Eliminates dead and redundant states
Register Retiming	Balances negative slack between registers
Expanded RAM / ROM Inference	Improves area by better utilizing dedicated RAM resources
Intermodule boundary optimization	Improves performance in critical paths that cross modules
Timing driven IOB mapping	Maximized IO performace while not sacrifisin max frequency
Timing driven driver sizing	Maximizes IO chip performance
Timing driven Tri-state optimization	Improves performance on internal tri-state busses
Improved High-Level RTL optimizations	Improves performance through high-level logic structures

Enhanced optimization control for advanced users

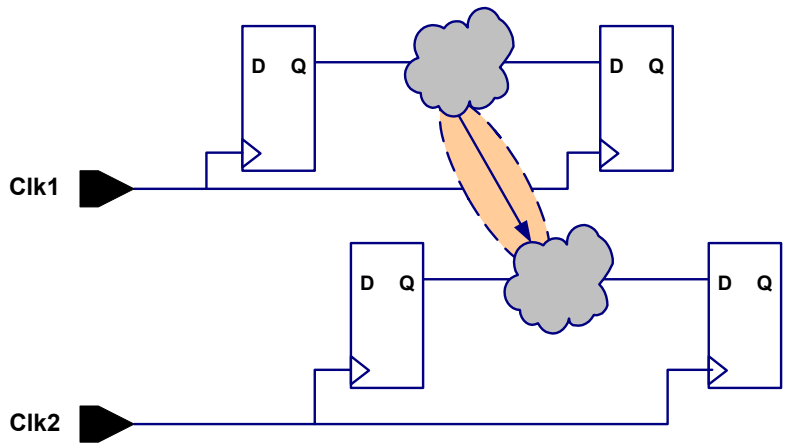
- **Precision provides more extensive and more precise control over the optimization process**
  - **Precision allows optimization control to be performed at the netlist object, module or global level**
  - **LeonardoSpectrum typically limited to coarse, global optimization control**

Control Feature	Leo Spec	Precision
RAM Implementation	X	X
ROM Implementation	X	X
Tri-state to Mux conversion	X	X*
Fanout	X	X*
Hierarchy Group	X	X
Hierarchy Flatten	X	X
Hierarchy Preserve	X	X
Multiplier Implementation	X	X*
IO Register mapping	X	X*
Preserve Signal	X	X
Preserve Driver	X	X
Optimize for Area / Delay	X	X
Don't Retime		X*
Register clock enable	X	X
Add IO Pad	X	X
Transform Set / Reset FF's	X	X
FSM Encoding	X	X*
Rad Hard Method		X*

**** Indicates enhanced optimization control***

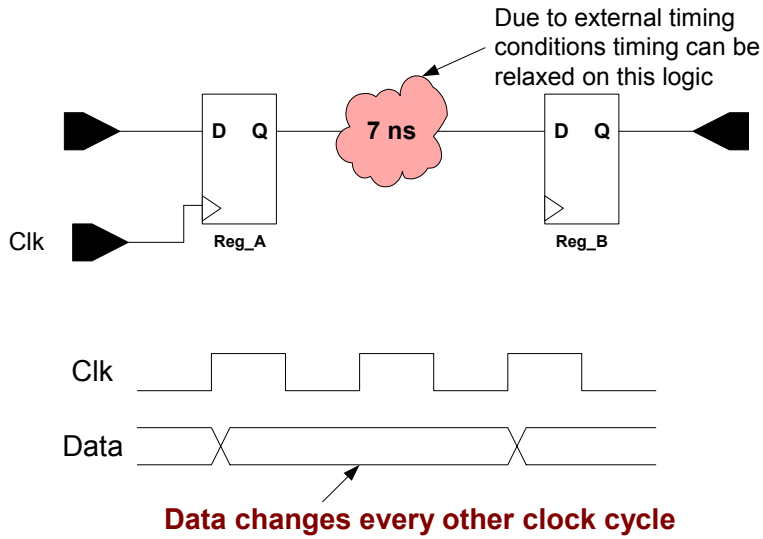
Detects all Critical Paths in Complex Designs

- **Precision includes new timing analysis that detects all critical paths in complex designs**
  - Supports multiple clocks in both synchronous and asynchronous clock domains
  - Automatically propagates clocks through gates and clock manager cells
- **Precision helps insure that critical paths are not undetected due to incomplete or incorrect constraints**
  - ***report missing constraints***
  - ***report clock domain crossing***
  - ***report clock source path***
- **LeonardoSpectrum is not capable of analyzing designs with complex clocking schemes**
  - Limited support for multiple clocks
  - Does not propagate clocks through clock manager cells
  - Does not offer constraint verification reports



Allows Constraints to reflect true designer intent

- **Precision fully supports "exception constraints" to allow designers to alter timing analysis to reflect true designer intent**
- **"Exception constraints" include:**
  - ***"false_path"***
  - ***"multicycle_path"***
  - ***"set_max_delay"***
- **LeonardoSpectrum offers only limited support for multi-cycle path**



Precision RTL vs. LeonardoSpectrum

Design Analysis

Analysis Feature	Leo Spec	Precision	Benefit
Interactive timing analysis	X	X	Provides "what-if" timing analysis
Multiple clock analysis		X	Finds true critical paths in complex designs
Asyncronous clock support		X	Eliminates false paths due to async clocks
multicycle path	partial	X	Lets users eliminate multi-cycle paths
false path		X	Lets users eliminate false paths
set_min_delay		X	Lets users easily override derived constriants
Missing constraint report		X	Insures that no timing errors go indectecte
Clock domain crossing report		X	Insures that async clocks are correct
PLL / DCM clock propagation	partial	X	Eliminates the need to set internal constraints
Internal clock detection	partial	X	Finds and reports all clocks
Clock propagation through cells		X	Eliminates the need to set internal constriants
Automatic constraint generation		X	Ease of use
View critical path	X	X	Clearly displays logic on critical path
View multiple critical paths		X	Understand relationships between multiple paths

- **Precision's capabilities match or exceed LeonardoSpectrum**

Summary

- **Precision RTL Synthesis addresses new requirements for today's complex FPGA designs**
  - **Intuitive operation improves ease of use**
  - **Accurate analysis helps users understand synthesis results**
  - **Excellent results achieves timing closure with fewer iterations**

The Precision Design Center