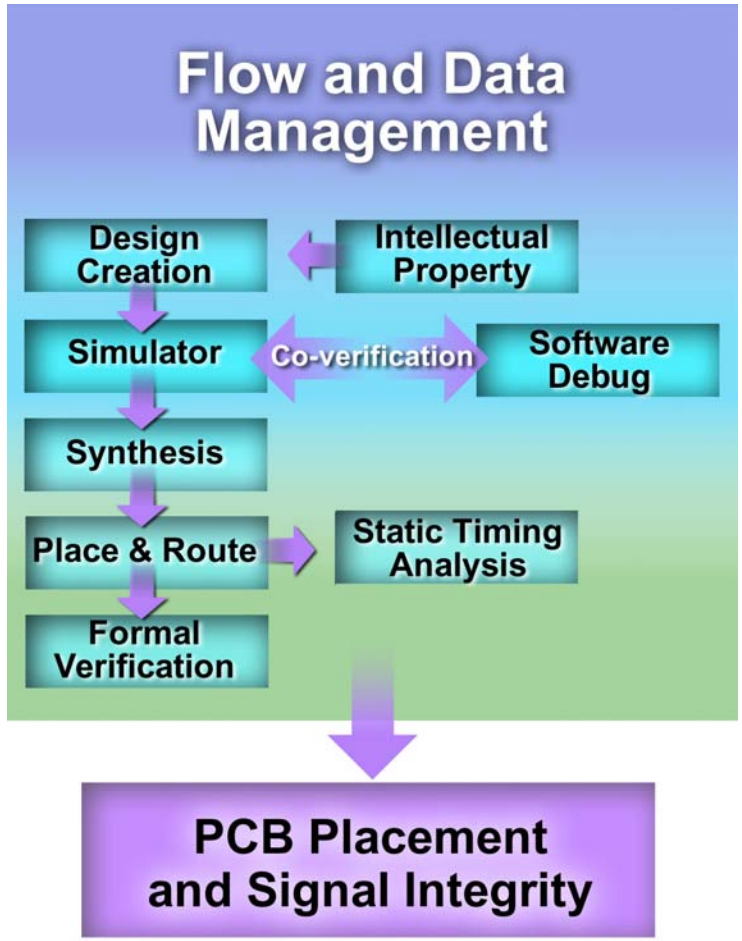
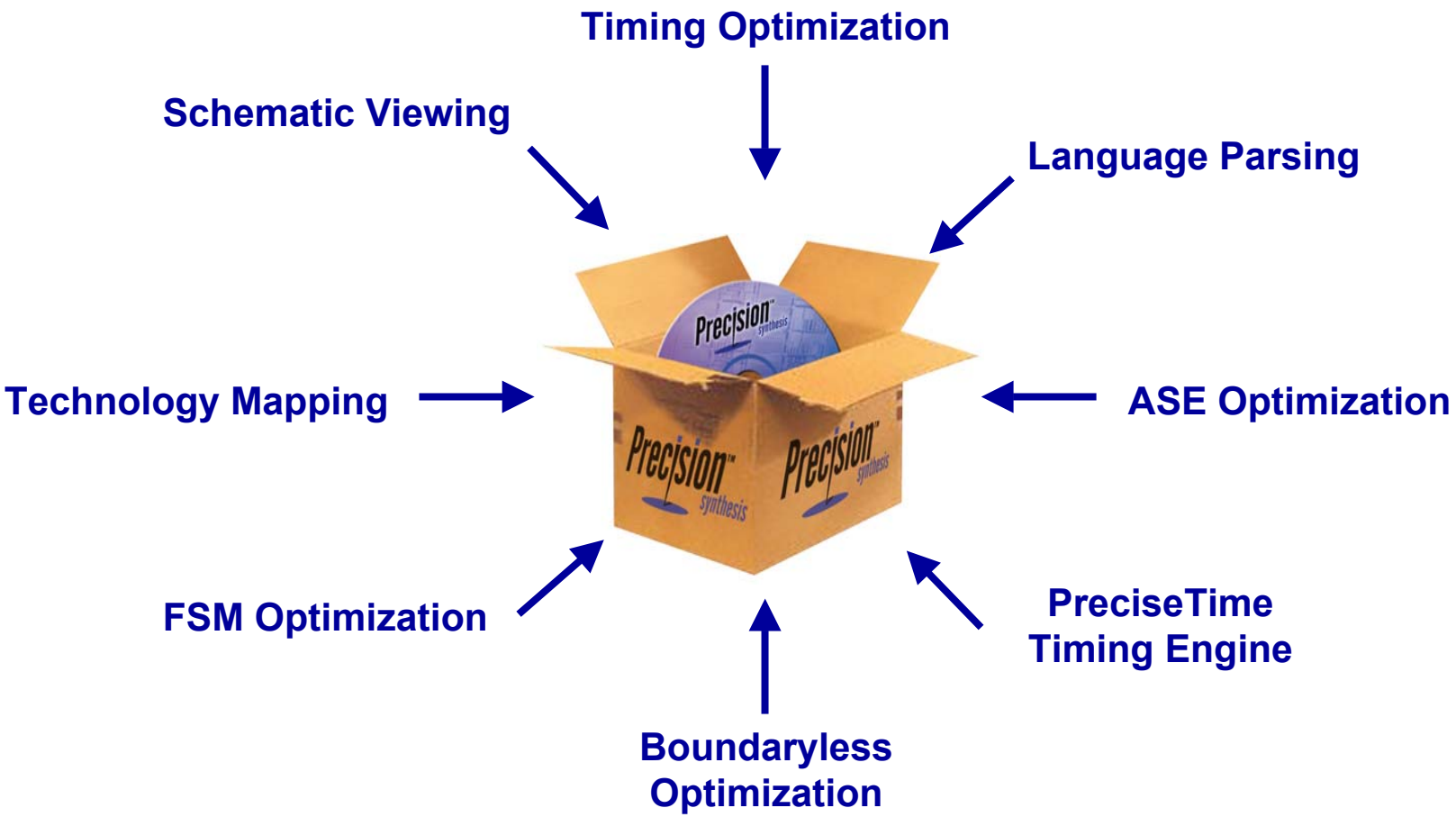
Precision RTL Synthesis
Technical Product Overview

#1 Provider of FPGA Design Solutions

- Data Management
- Design Creation
  - Graphical, Text, IP
- Verification
  - Simulation
  - Formal
  - HW/SW Co-verification
  - Software Debug
  - Direct System Verification
- Analysis
  - Signal Integrity
  - Timing Analysis
- Synthesis
  - High Level Synthesis (HLS)
  - RTL Synthesis
  - FPGA Optimization
  - Physical Synthesis
- Flows



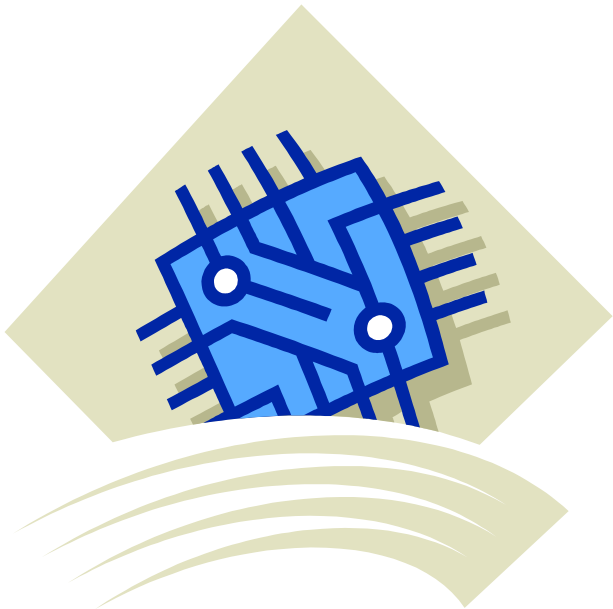
Built upon a decade of experience



- **20,000 synthesis licenses in use today**

The FPGA Design Challenge

- **FPGA designers are being asked to perform increasingly complex designs while maintaining a broad range of design responsibilities**



The Precision Synthesis Solution

- **Precision solves this challenge by providing a FPGA synthesis environment that is intuitive to use, flexible and provides excellent results with a pushbutton flow**

Agenda

- Intuitive Use
- Excellent Results with pushbutton Flow
- Broad design methodology support
- Accurate Analysis to drive performance
- Product Roadmap

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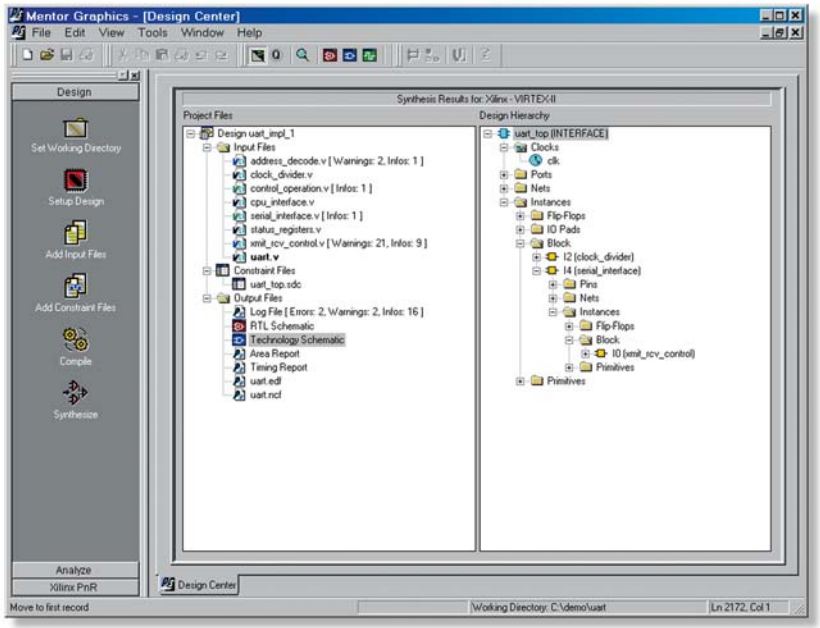
Precision Design Center

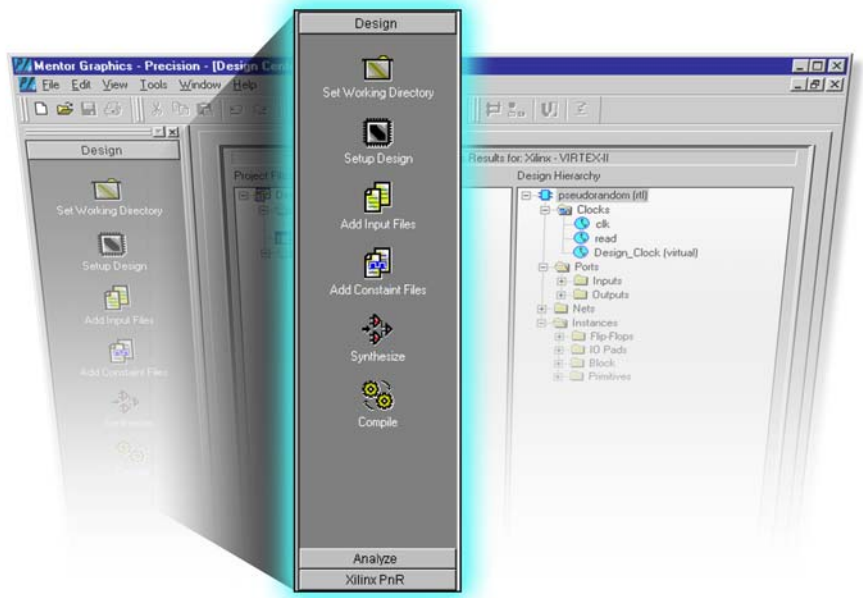
- **A single interface drives the complete synthesis process**
- **Includes advanced functionality required for large designs**

The Synthesis Design Center



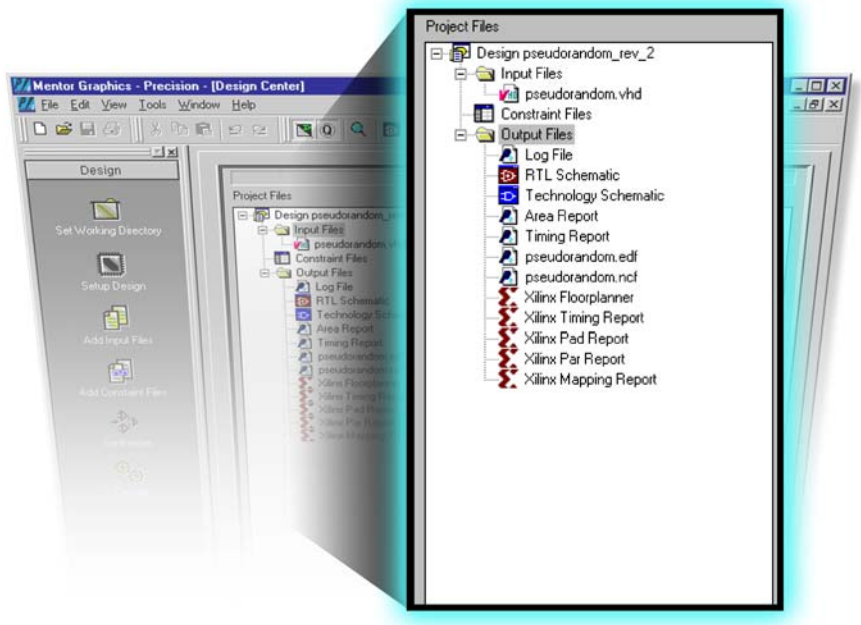
Synthesis Design Bar

- **Precisions Design Bar guides users step-by-step through the synthesis process**



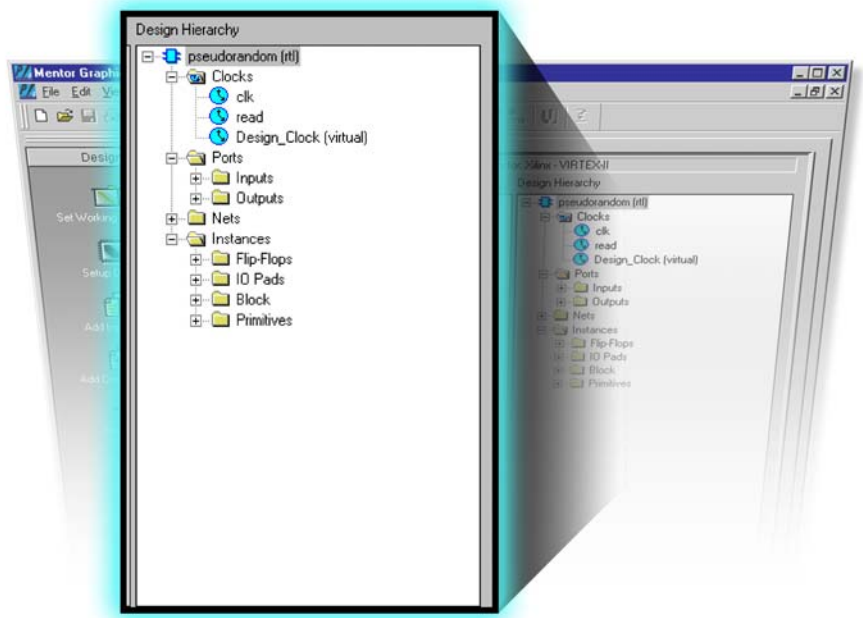
Project Management

- **The Project Browser manages all synthesis input and output files**



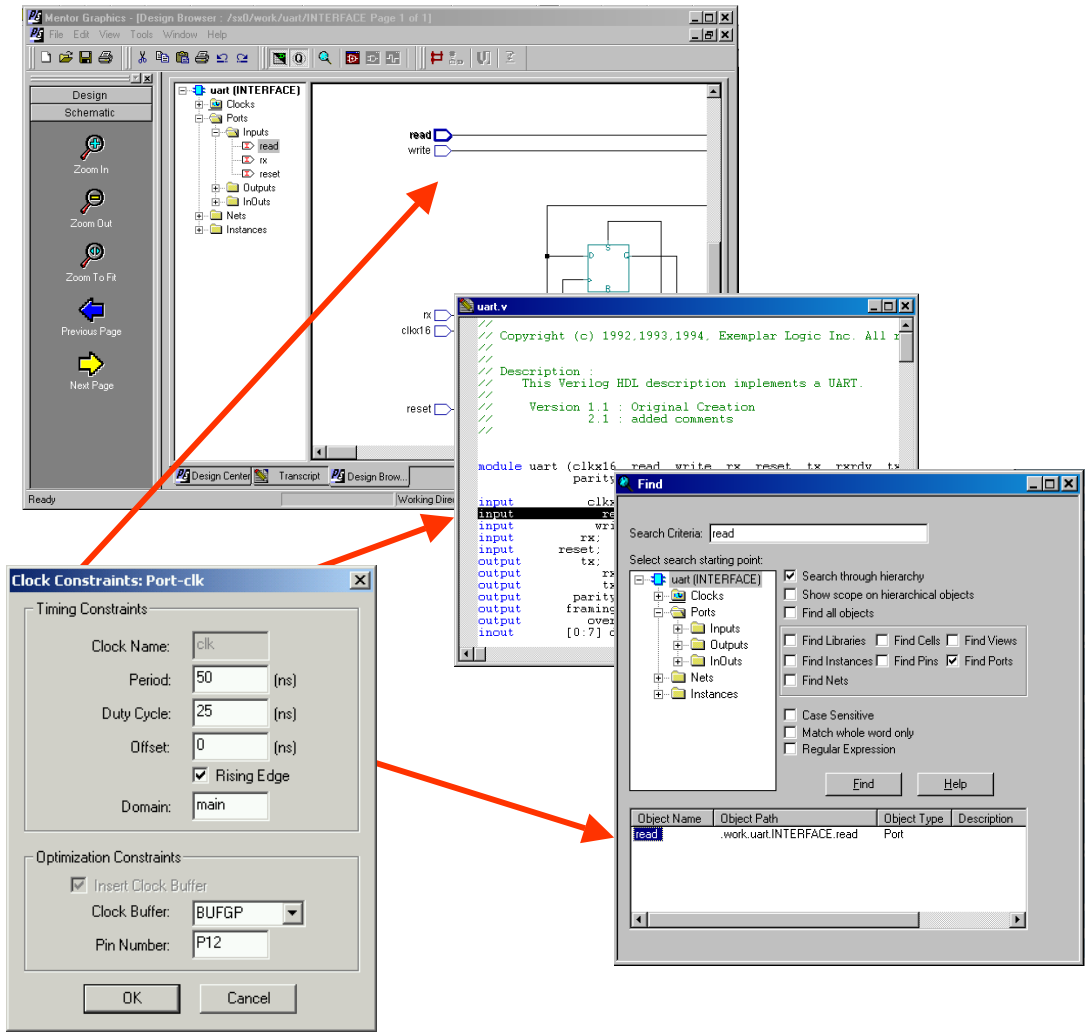
Design Hierarchy Browser

- **The Design Hierarchy Browser provides an easy means to view and analyze design results**



Flexible Constraint Entry

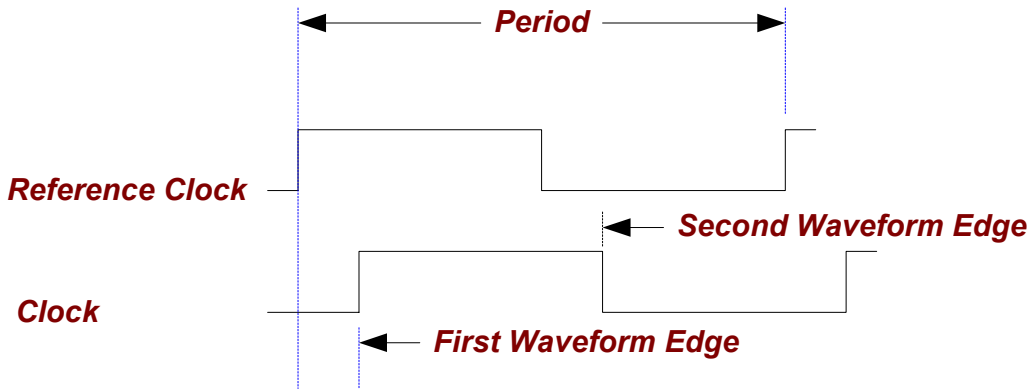
- Precisions allows design constraints to set throughout the user interface
- Even complex constraint files can be quickly created



Constraints based on Industry Standards

- **Industry expertise is leveraged through the support of Synopsys Design Constraints (SDC) for specifying timing in a design**

```
# Clock Constraints
create_clock clk -period 10 -domain main

# Input Constraints
set_input_delay 2 data_en -clock clk
set_input_delay 3 data_in* -clock clk

# Output Constraints
set_output_delay 3 data_stb -clock clk
set_output_delay 8 data_out* -clock clk
```



Intuitive Synthesis Scripts

- **Users only need to learn 4 synthesis commands**

The **"setup_design"** command is used to configure details about how synthesis is performed

The **"add_input_file"** command adds all input files including constraint, RTL, SDF, EDIF.

The **"compile"** command will read the RTL files into memory

The **"synthesize"** command will perform optimization and generate all netlists and report files

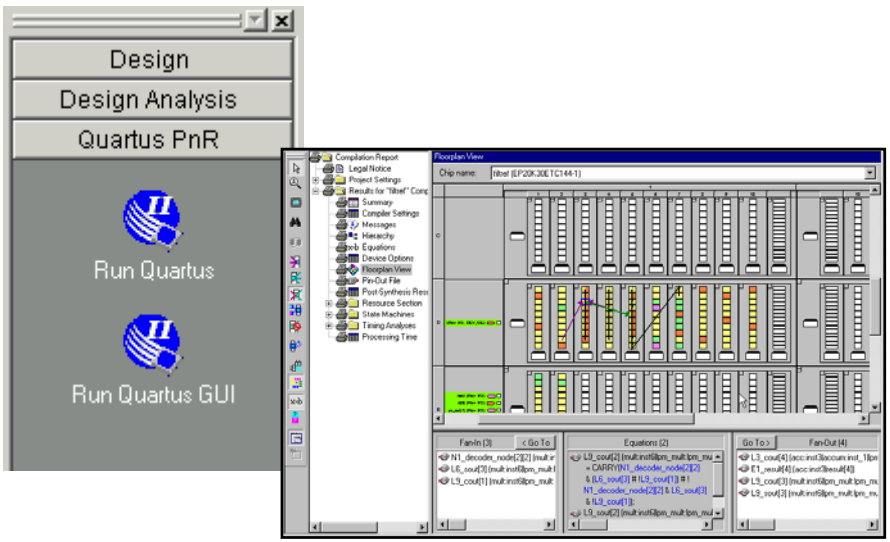
Precision Script File

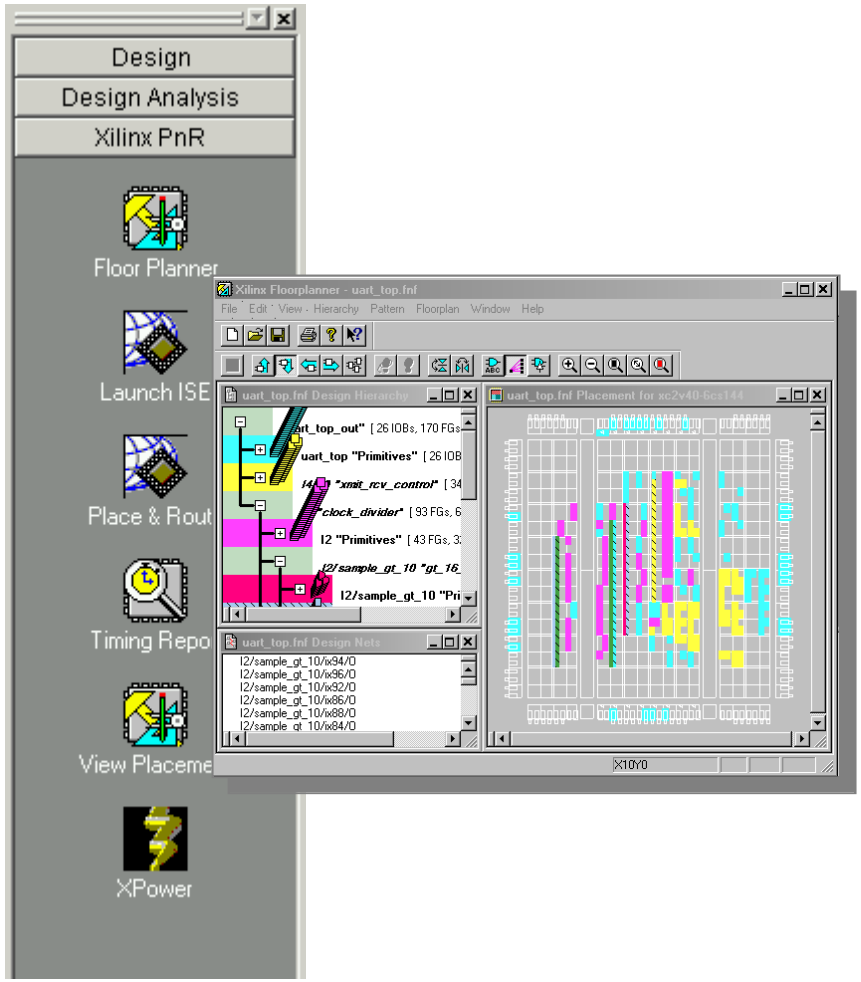
```
# Setup Technology Environment
setup_design  -manufacturer "Xilinx"
setup_design  -family "VIRTEX-II"
setup_design  -part "2V40cs144"
setup_design  -speed "6"

# Add input files
add_input_file {traffic.v}

# Setup timing constraints
setup_design -frequency 62.5

# Complete the optimization process
compile
synthesize
```


Company Confidential, 2003 Mentor Graphics Corp

Pushbutton Place and Route Integration

- Perform place and route with a single mouse click
- Precision creates vendor constraint files





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- **Excellent Results with pushbutton Flow**
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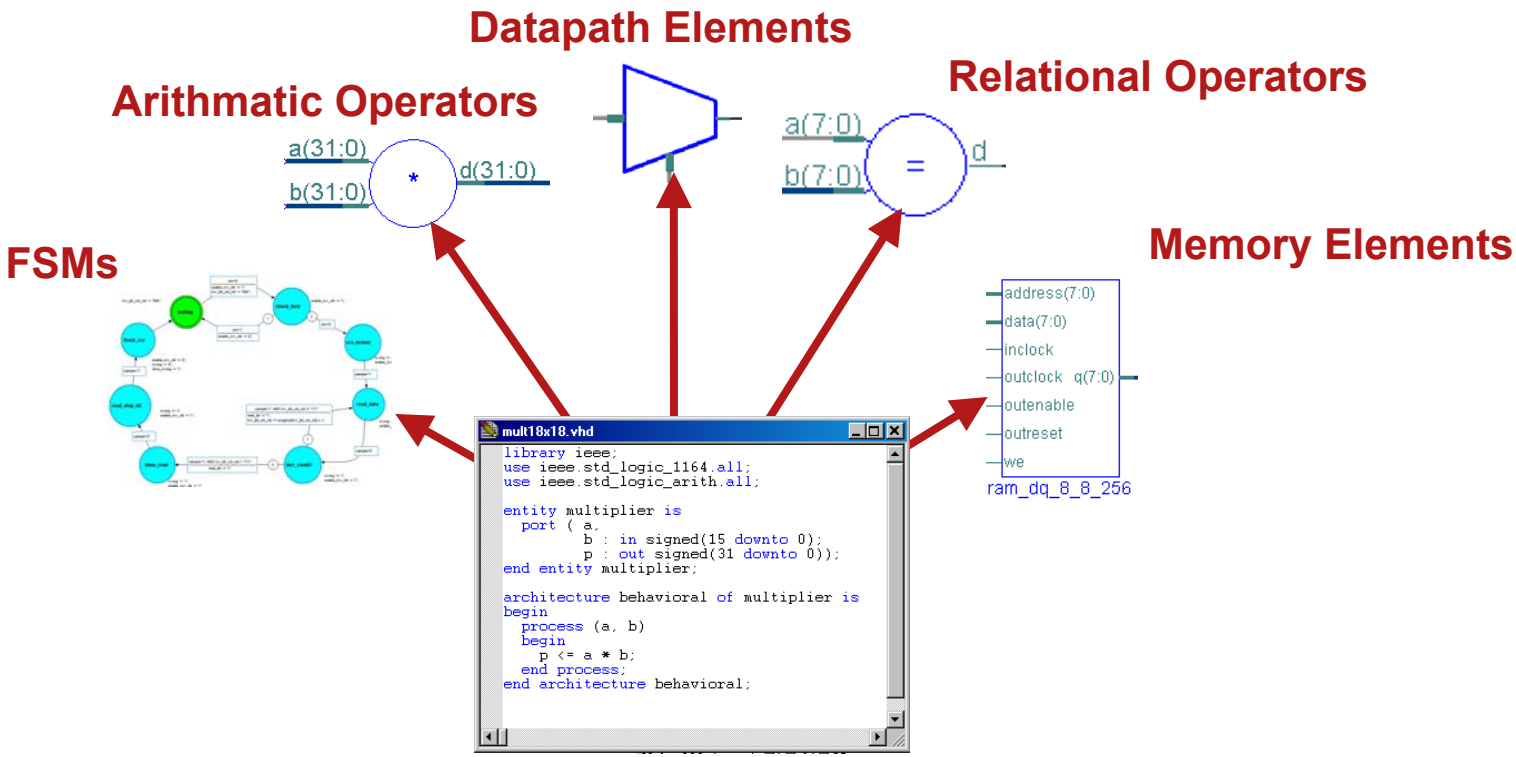
High-Level Extraction

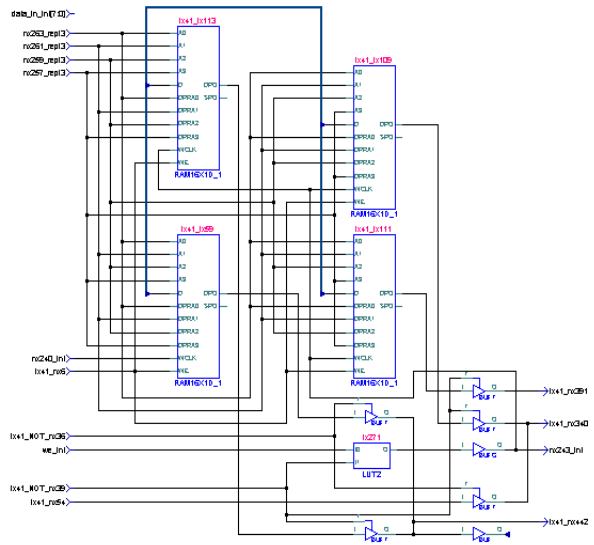


- **Precision obtains excellent results by identifying and extracting high level design elements.**

Architecture Signature Extraction

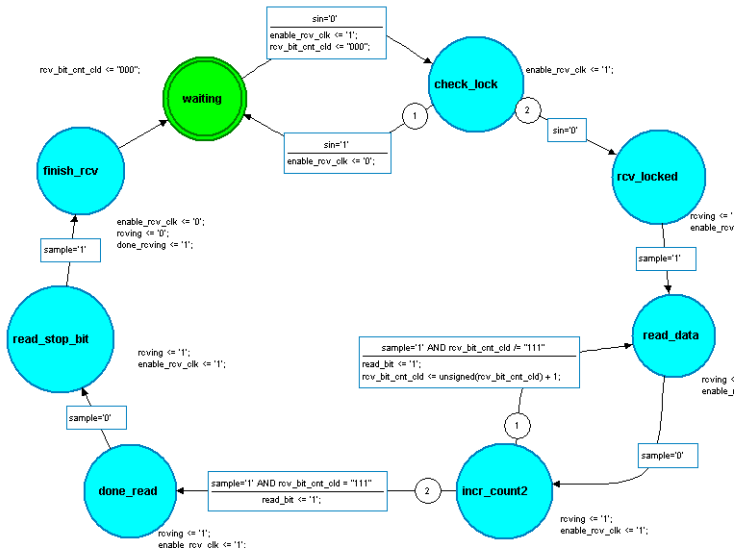
- Precisions ASE algorithms automatically map RTL structures to FPGA architectures
- Designers do not need to know the details of an FPGA device

```
Data_out <= mem_array(address)
```



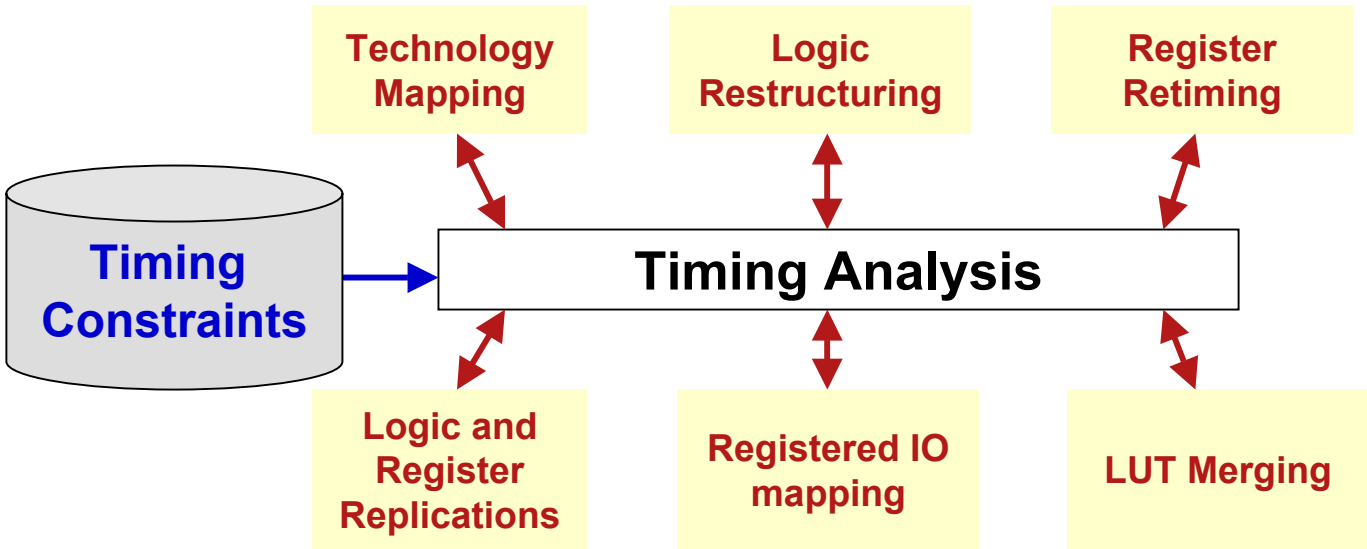
Leading FSM Optimization

- **Extensive Recognition**
  - **Precision detects FSMs from enumerated types, constants, pragmas and ‘defines**
- **Industry Leading Analysis**
  - **Precision detects unreachable, equivalent and terminal states**
- **Advanced Optimization**
  - **Precision is the only synthesis tool that automatically removes unreachable states and merge equivalent states**



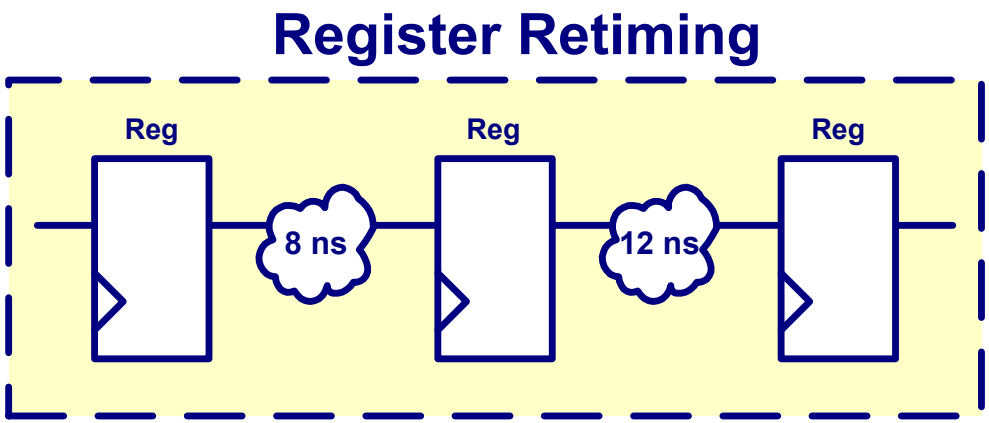
Constraint Based Optimization

- Optimization is configured based on the design and user defined timing constraints
- Users need to know the requirements of their designs, not their synthesis tool or device architectures



Boundaryless Optimization

- Automatically moves logic across operators, registers and module boundaries when necessary to meet timing constraints.
- Precisions "Boundaryless Optimization" technology overcomes traditional barriers to high-performance implementations without user intervention



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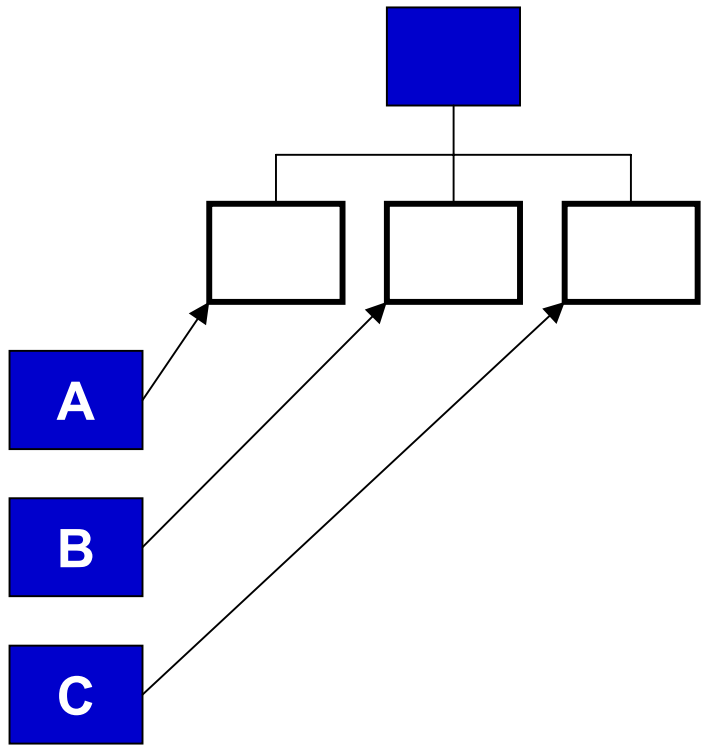
Flexible Design Methodology Support

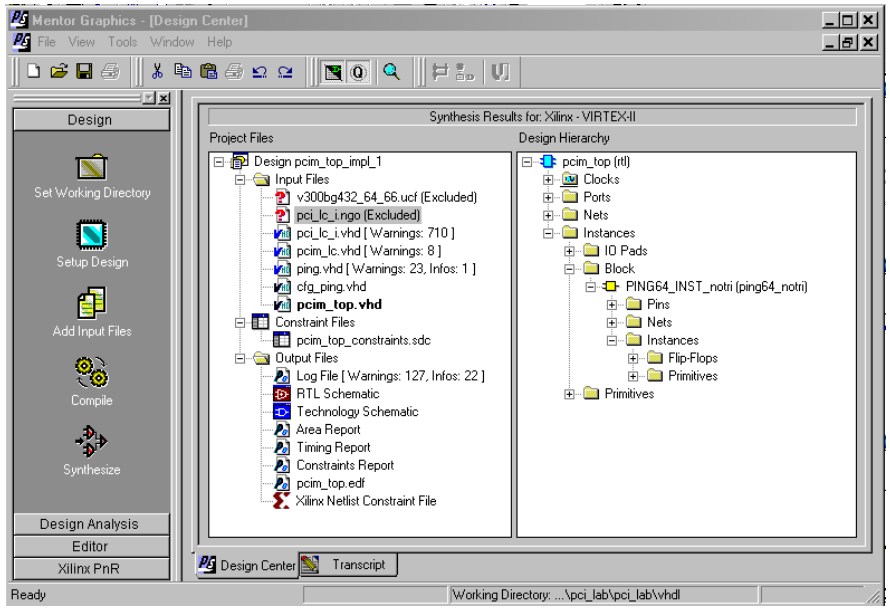
- **Precision supports for both top-down and block-based design methodologies allowing designers to work in the flow they feel most comfortable**



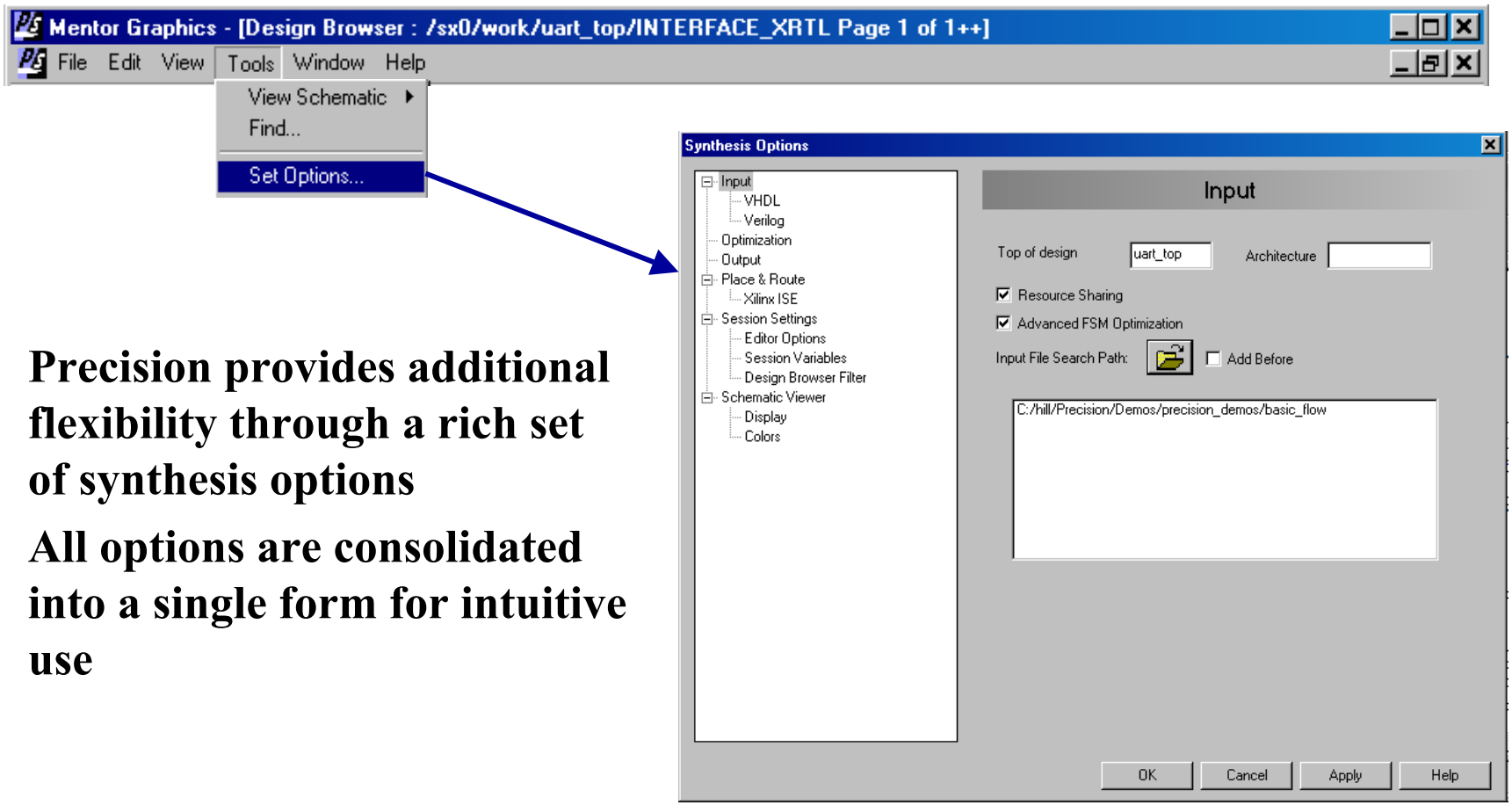
Automated Design Flows

- **Precision makes complex FPGA design flows easy to use**
  - **Contains built-in automation for important design flows such as the Xilinx PCI core**

Xilinx PCI Core



Synthesis Options



- **Precision provides additional flexibility through a rich set of synthesis options**
- **All options are consolidated into a single form for intuitive use**

The Precision Synthesis Solution

- Intuitive Use
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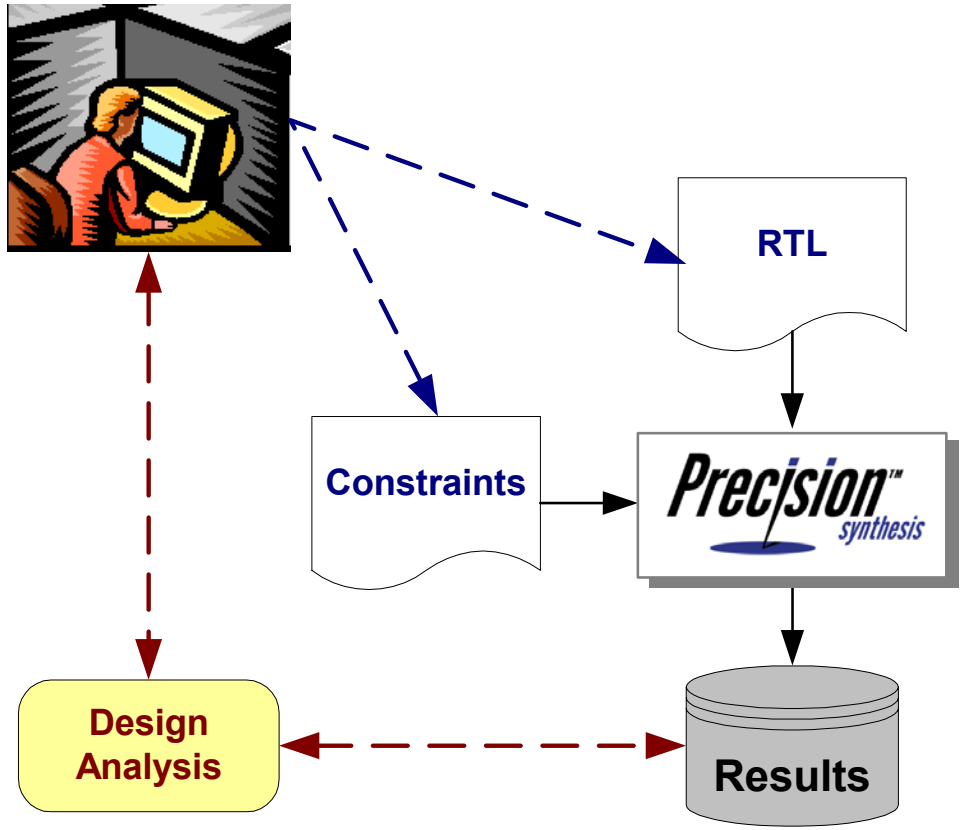
Design Analysis Improves Synthesis Inputs

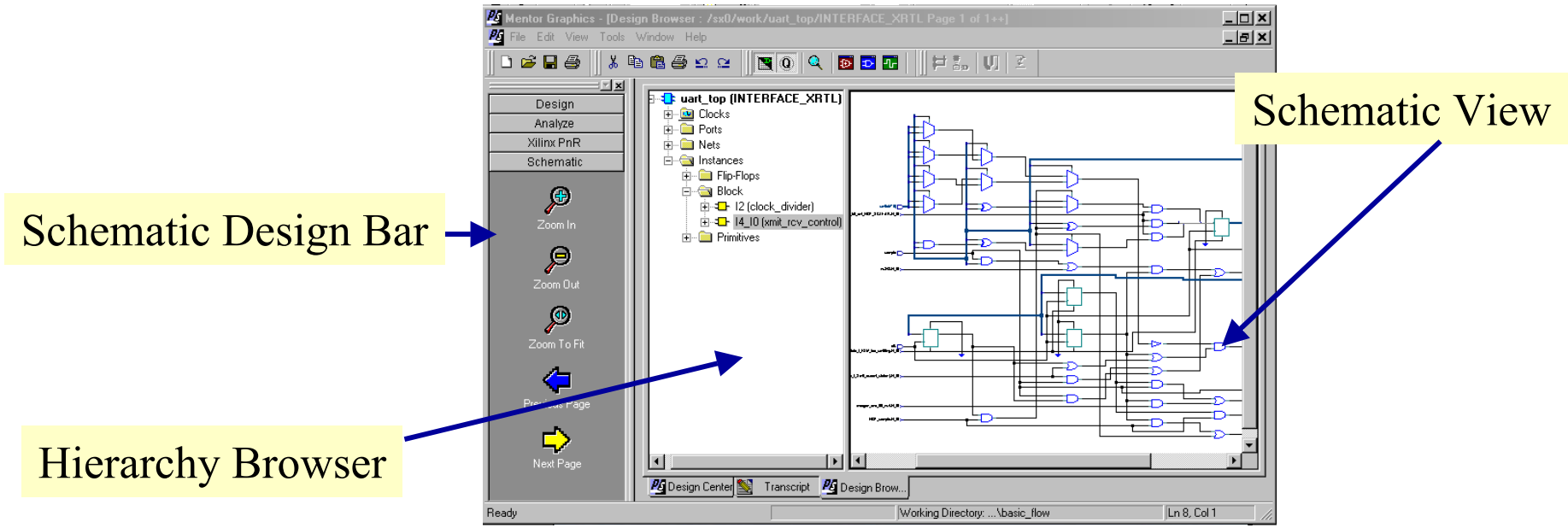
- Synthesis results are directly effected by input RTL and constraint files
- Design Analysis enables a designer to make improvement to these inputs



Precision Design Analysis

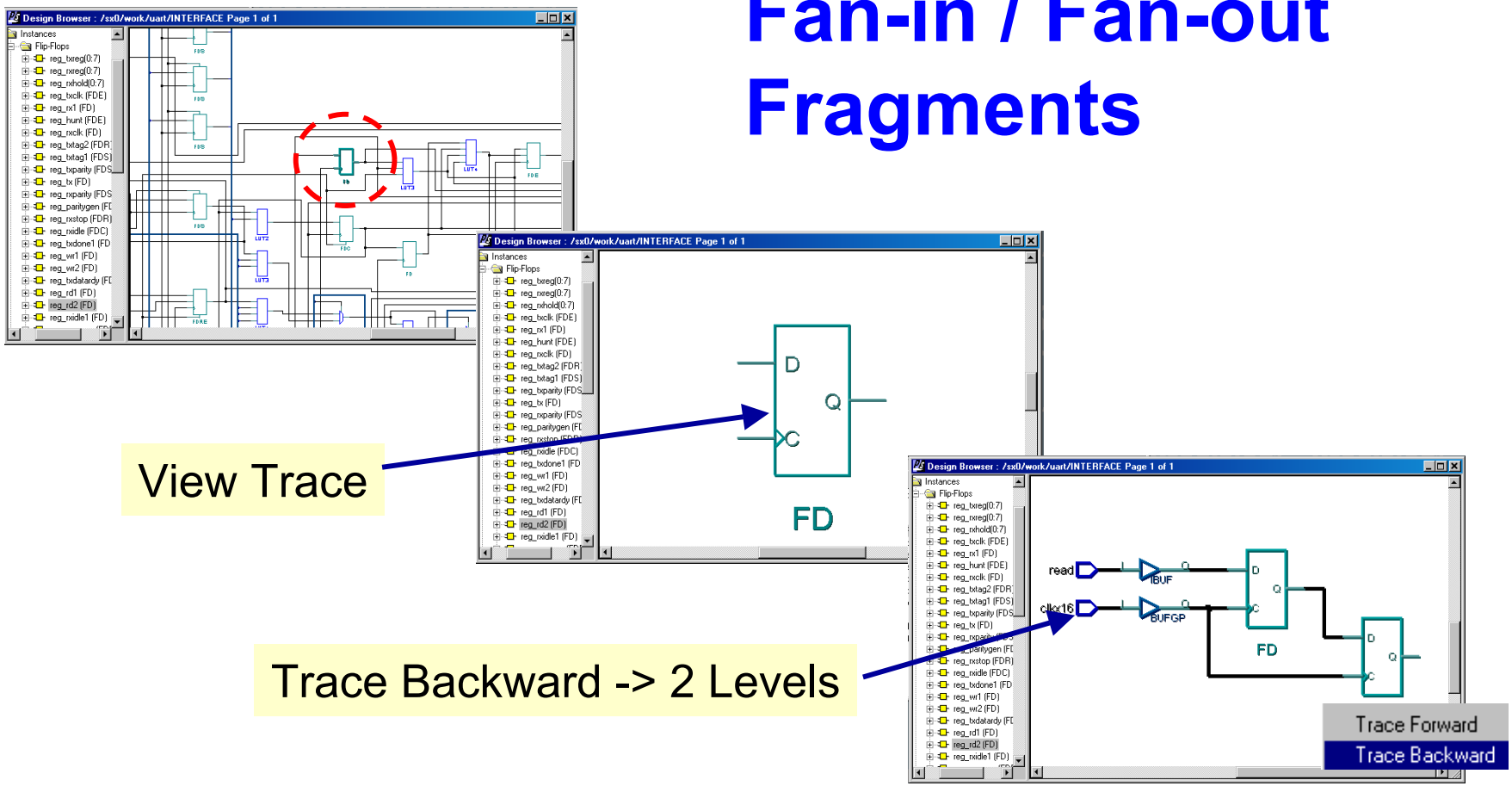
- **Precisions "Analyze" Design Bar provides quick access to a rich set of design analysis features**

Built-in Schematic Viewing



- **Precisions integrated schematic viewer provides a clear visualization of the synthesis process.**
  - **High-level RTL schematics help a designer determine the impact of coding**
  - **Technology schematics show where and how device specific resources such as RAM and ROM are utilized.**

Fan-in / Fan-out Fragments

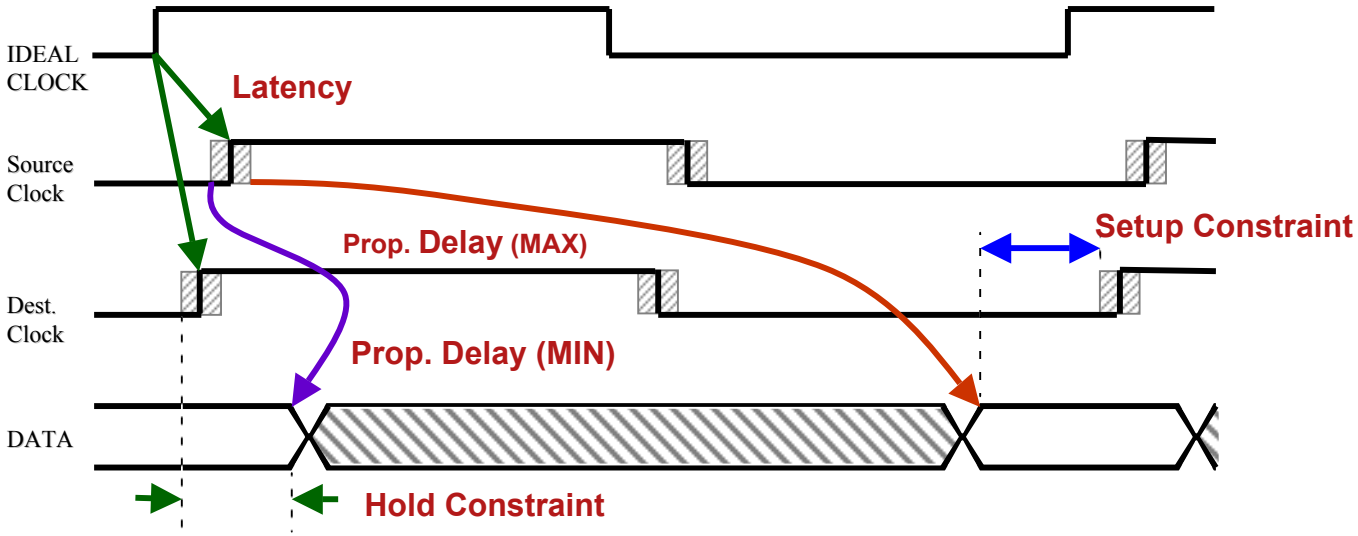


View Trace

Trace Backward -> 2 Levels

- **Filter on any selected net or instance**
- **Trace forward or back from any selected net or instance**
- **Incrementally grow filtered schematic with a double-click**

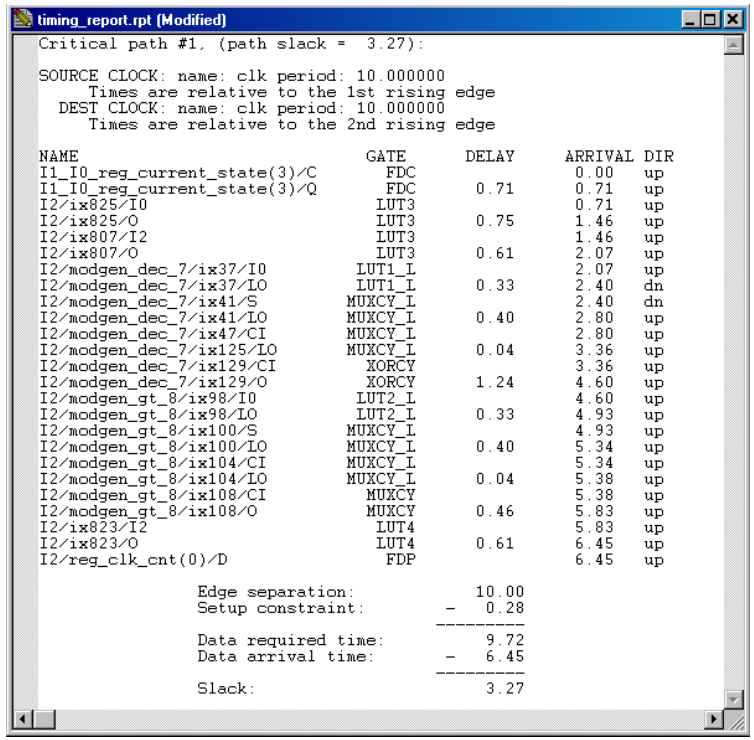
Accurate Timing Analysis



- Precision 's PreciseTime™ timing analysis finds the true critical paths in even the most complicated designs and clocking schemes.
- Based on timing engine from Mentor Graphics Velocity product
  - ASIC golden signoff timing analysis

Interactive Timing Path Reports

- Precision supports fully interactive timing analysis
- Multiple reports can be generated on any specified paths without rerunning optimization



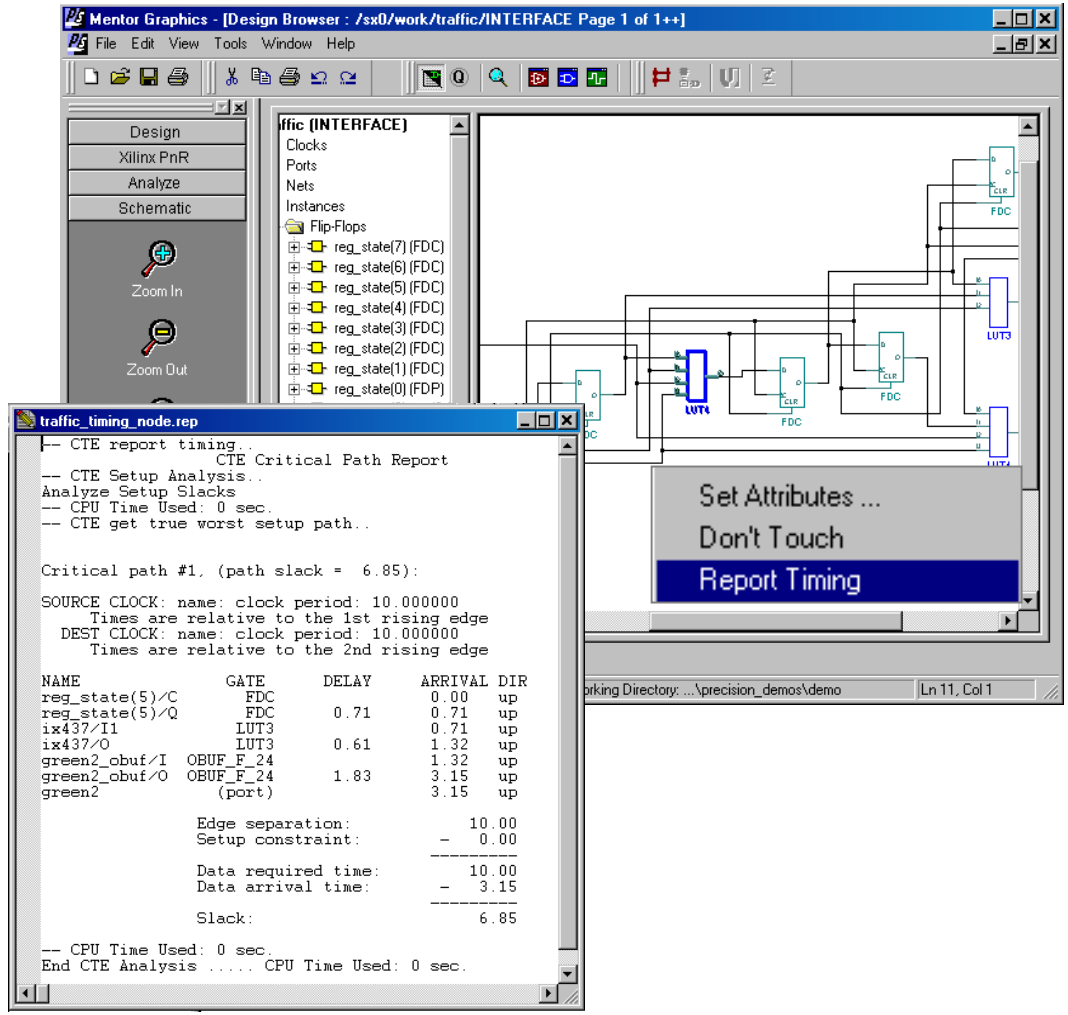
timing_report.rpt [Modified]

```
Critical path #1, (path slack =  3.27):

SOURCE CLOCK: name: clk period: 10.000000
     Times are relative to the 1st rising edge
  DEST CLOCK: name: clk period: 10.000000
     Times are relative to the 2nd rising edge

NAME                                GATE      DELAY     ARRIVAL DIR
I1_I0_reg_current_state(3)/C         FDC                  0.00   up
I1_I0_reg_current_state(3)/Q         FDC       0.71       0.71   up
I2/ix825/I0                         LUT3                 0.71   up
I2/ix825/O                          LUT3       0.75      1.46   up
I2/ix807/I2                         LUT3                 1.46   up
I2/ix807/O                          LUT3       0.61      2.07   up
I2/modgen_dec_7/ix37/I0           LUT1_L                 2.07   up
I2/modgen_dec_7/ix37/LO           LUT1_L       0.33      2.40   dn
I2/modgen_dec_7/ix41/S            MUXCY_L                2.40   dn
I2/modgen_dec_7/ix41/LO           MUXCY_L      0.40      2.80   up
I2/modgen_dec_7/ix47/CI           MUXCY_L                2.80   up
I2/modgen_dec_7/ix125/LO          MUXCY_L      0.04      3.36   up
I2/modgen_dec_7/ix129/CI            XORCY                3.36   up
I2/modgen_dec_7/ix129/O             XORCY      1.24      4.60   up
I2/modgen_gt_8/ix98/I0            LUT2_L                 4.60   up
I2/modgen_gt_8/ix98/LO            LUT2_L       0.33      4.93   up
I2/modgen_gt_8/ix100/S            MUXCY_L                4.93   up
I2/modgen_gt_8/ix100/LO           MUXCY_L      0.40      5.34   up
I2/modgen_gt_8/ix104/CI           MUXCY_L                5.34   up
I2/modgen_gt_8/ix104/LO           MUXCY_L      0.04      5.38   up
I2/modgen_gt_8/ix108/CI             MUXCY                5.38   up
I2/modgen_gt_8/ix108/O              MUXCY      0.46      5.83   up
I2/ix823/I2                          LUT4                5.83   up
I2/ix823/O                           LUT4      0.61      6.45   up
I2/reg_clk_cnt(0)/D                   FDP                6.45   up

                Edge separation:              10.00
                Setup constraint:           -  0.28
                                            ---------
                Data required time:           9.72
                Data arrival time:          -  6.45
                                            ---------
                Slack:                        3.27
```

```
Report_timing -to I2.reg_clk_cnt(0).D -num_paths 3 -show_schem
```

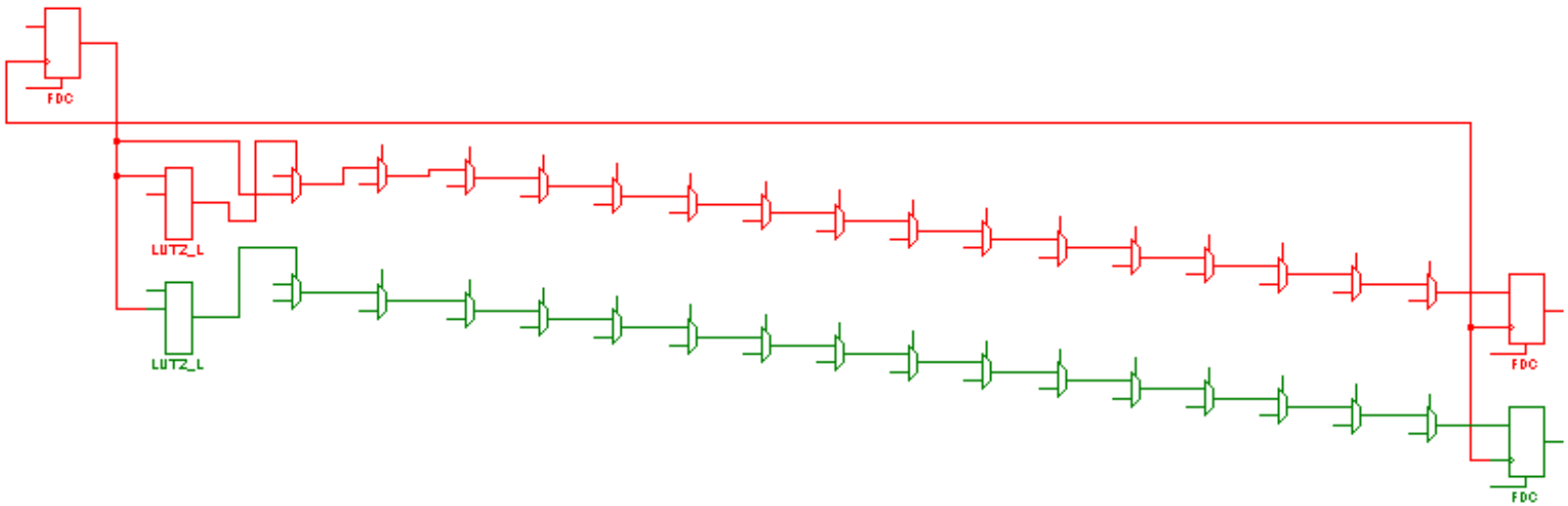
Timing Reports from the Schematic

- **Designers can initiate timing reports from any selected netlist instance or port in the user interface**
- **Precision allows designers to explore the design from many angles**



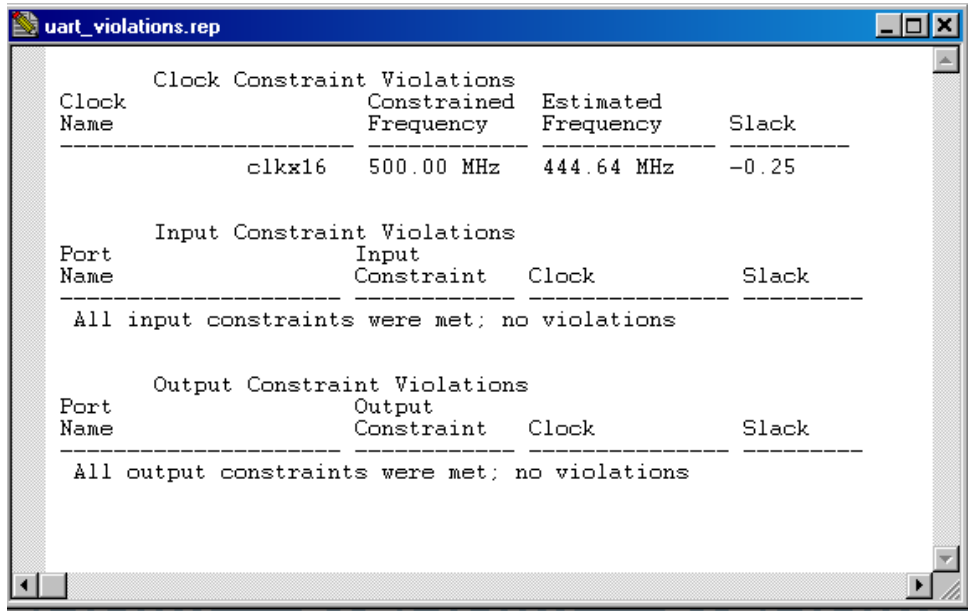
Critical Path Viewing

- **Precision allows designers to easily analyze their most critical logic by creating filtered schematics of timing paths**

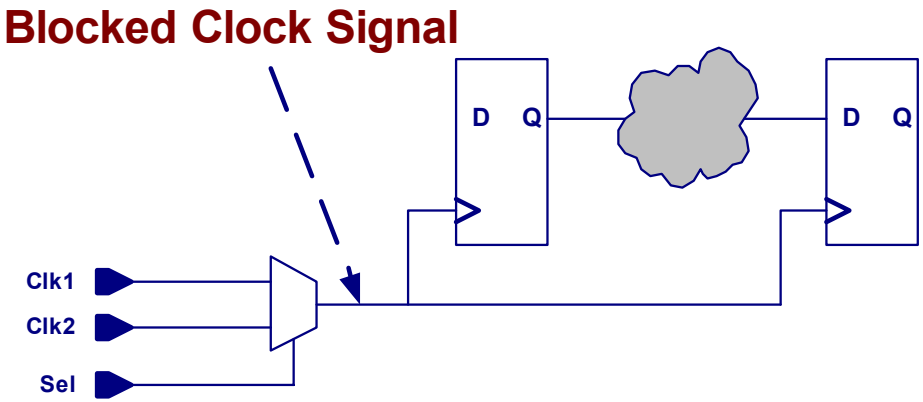


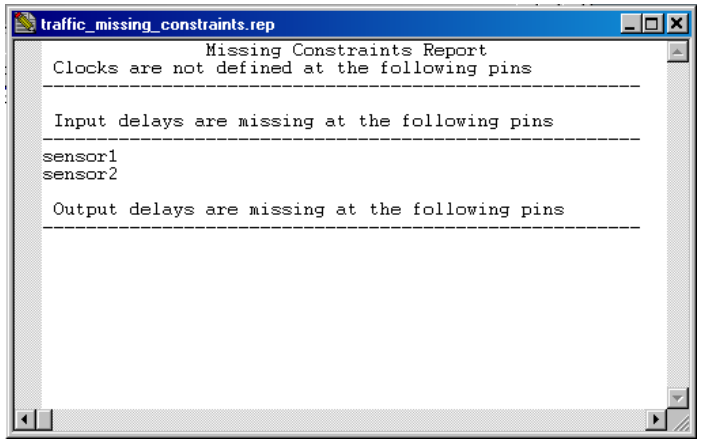
Timing Violations Report

- **Precisions Timing Violations report quickly identifies which specific timing constraints are not meeting timing**



Constraints Analysis

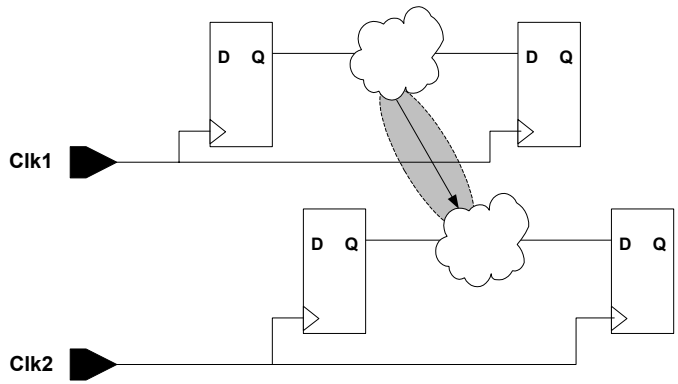




- **Precision eliminates unnecessary schedule risk by performing a complete constraint analysis prior to synthesis to insure that designs are fully and accurately constrained**

Clock Domain Analysis

- Key analysis feature that identifies timing paths between clocks of different domains
- Allows users to verify that clock domains are truly isolated or that inter-domains paths are designed with metastable tolerant design techniques




```
> Report_timing -clock_domain_crossing
```

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The Precision Synthesis Platform

- **Precision is a synthesis technology platform designed to address the entire synthesis problem**