WHITE PAPER

Precision RTL Synthesis supports clock propagation across PLLs

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PLL Support

The new generations of Altera® PLDs (Stratix™ GX, Cylcone™, APEX™ II) offer PLLs (enhanced and fast) for clock synthesis purposes. The embedded PLL blocks in the Stratix device are high-performance clock management units that offer a host of features that were previously found only in high-end discrete PLL devices. Apart from the basic PLL features like clock multiplication, clock division and phase-shift, the PLLs found in Stratix offer features like spread-spectrum clocking, clock switchover and programmable delay shift. With the capability to support these features, the Stratix PLL is designed to function as a central clock manager for a system.

When a PLL is used in a design, the challenge faced by a synthesis tool is to automatically propagate the clock through to the output of the PLL. The traditional method requires user intervention to set the output clock (and its values) of the PLL. In designs using multiple PLLs, this translates to a higher potential of introducing an error. Precision™ RTL Synthesis automates this process of propagating the clock, thus significantly reducing user intervention and increasing the accuracy of the design's timing analysis. When a PLL is instantiated in a design, Precision RTL Synthesis is able to propagate the clock and also calculate its intended output value based on the attributes passed along with the component.

Instantiating PLL Megafunctions

A device family specific PLL megafunction can be created using Altera's MegaWizard® Plug-in Manager utility. The various modes of operation and options for the PLL megafunction can be set through the MegaWizard GUI. For the PLL megafunction created n the example below, the target technology is Altera's Stratix device. An *altpll* component serves the purpose of a PLL here.

A code snippet of the instantiated *altpll* component's mapping is shown in Figure 1. The various attributes define clock synthesis functions of the PLL. Precision RTL is capable of detecting the *altpll* component and consequently is able to extract the various attributes passed along with it. Figure 2 shows the post-synthesis technology view of the *altpll* component. A right mouse-over reveals that the various attributes have been passed along with this component.

```
altpll_component : altpll
GENERIC MAP (
    bandwidth_type => "AUTO",
    clk0_duty_cycle => 50,
    lpm_type => "altpll",
    clk0_multiply_by => 1,
    lock_low => 5,
    invalid_lock_multiplier => 5,
    inclk0_input_frequency => 5000,
    gate_lock_signal => "NO",
    extclk0_duty_cycle => 50,
    clk0_divide_by => 2,
    extclk0_phase_shift => "0",
    extclk0_divide_by => 9,
    pll_type => "AUTO",
    valid_lock_multiplier => 1,
    clk0_time_delay => "0",
    spread_frequency => 0,
    extclk0_time_delay => "0",
    operation_mode => "NORMAL",
    extclk0_multiply_by => 3,
    lock_high => 1,
    compensate_clock => "CLK0",
    clk0_phase_shift => "0"
```

Figure 1. *altpll* component

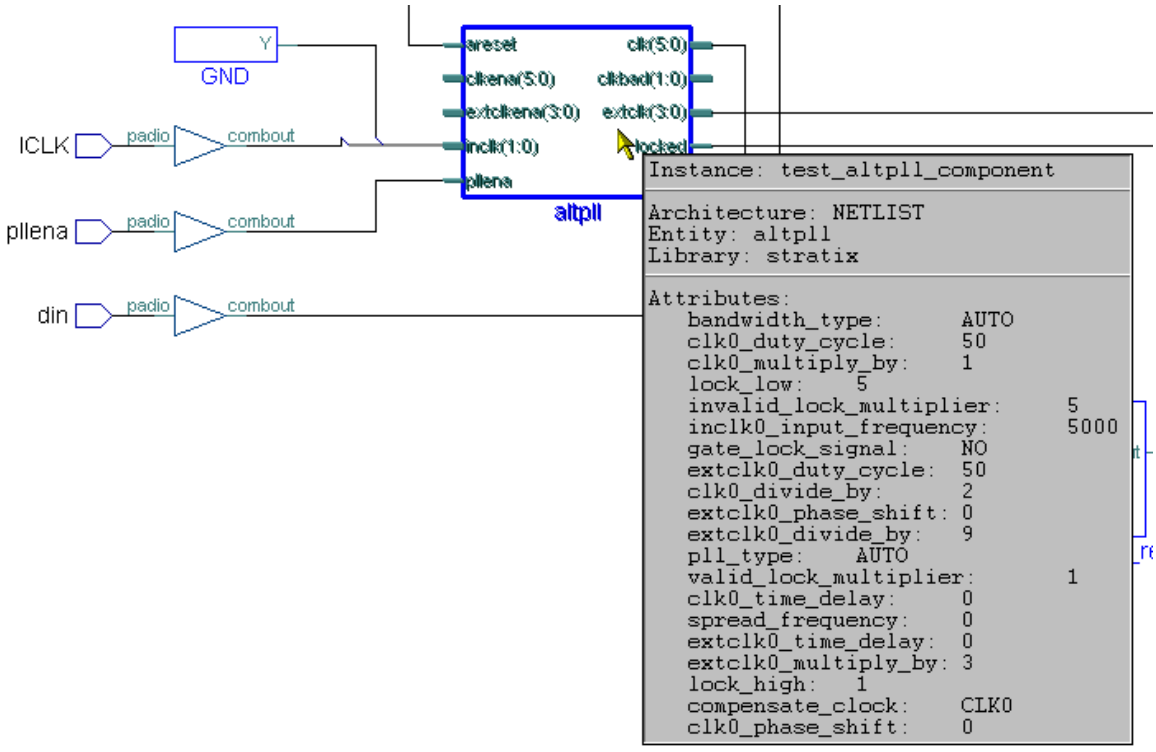

Figure 2—Precision RTL's technology view of the *altpll* component

Synthesis and Timing Analysis

After compile, Precision RTL extracts the primary input clock to the *altpll* component (ICLK in Figure 2) and displays it in the *Clocks* folder under the Design Hierarchy as shown in Figure 3.

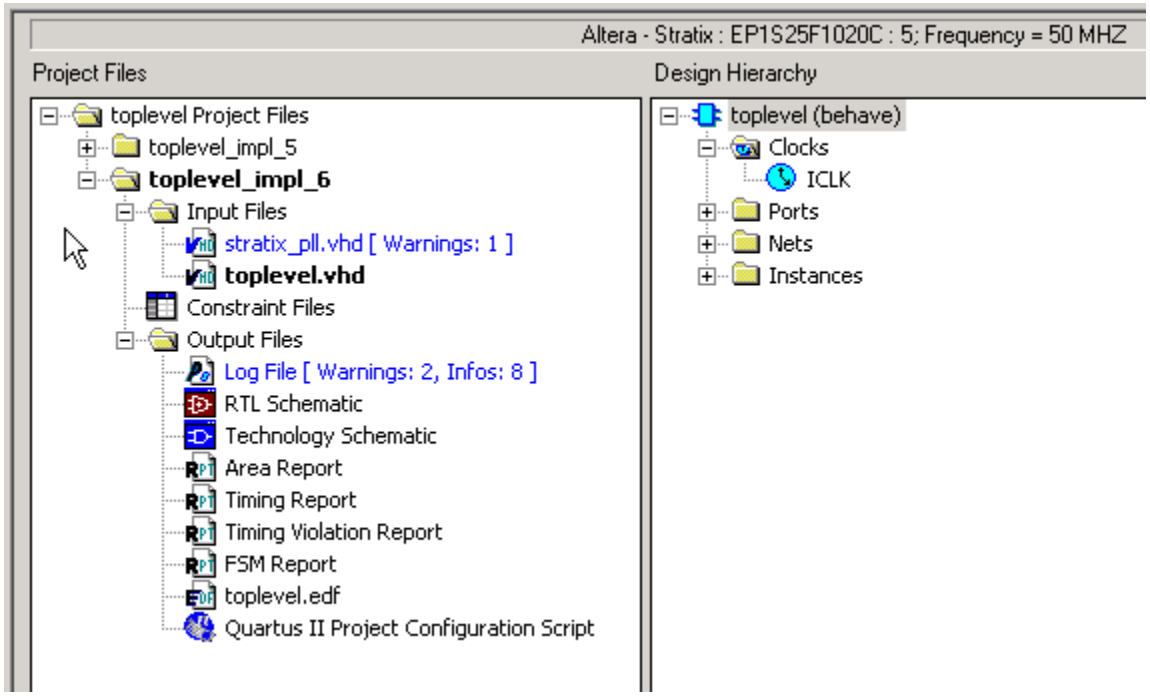

Figure 3—Primary input clock is extracted and displayed in the *Clocks* folder.

Figure 4 is an excerpt from the timing report and shows that the output clock, clk0 has a period of 10ns (100 MHz). This is the expected value after dividing the input clock (frequency of 200 MHz) by two. The timing report outlines the critical paths in the design. The slack reported by Precision RTL gives the user a realistic number for the timing for this design that uses a PLL. A final accurate timing result than then be obtained by placing and routing the design.

```
SOURCE CLOCK: name: test/altpll_component/clk(0) period: 10.000000
     Times are relative to the 1st rising edge
  DEST CLOCK: name: test/altpll_component/clk(0) period: 10.000000
     Times are relative to the 2nd rising edge

NAME                    GATE                 DELAY    ARRIVAL DIR
reg_qout_int/clk    stratix_lcell_reg                    0.00   up
reg_qout_int/regout stratix_lcell_reg        0.73        0.73   up
reg_qout/dataa      stratix_lcell_reg                    0.73   up

                Edge separation:                10.00
                Setup constraint:         -      0.50
                                          ----------
                Data required time:             9.50
                Data arrival time:        -     0.73
                                          ----------
                Slack:                          8.78
```

Figure 4—Snippet from Precision RTL generated timing report

Integrated Place and Route

Precision RTL's integrated place and route capability allows a user to run the post-synthesis netlist (EDIF) through Quartus II in a seamless environment. Upon completion of place and route, you can open the compilation report to verify the resource usage and timing. Figure 5 shows that the slack reported for a path is actually very close to what was estimated by Precision RTL. This close degree of estimation coupled with the capability to calculate timing across a PLL proves to be a critical time saving feature.

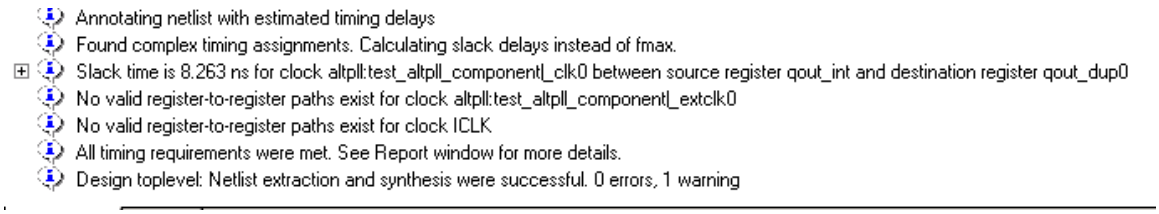

Figure 5—Excerpt from Quartus II compilation report

Conclusion

By supporting new features like PLLs that are being offered in the Stratix and Cyclone lines of Altera PLDs, Precision RTL is making it possible for designers to shorten their design cycles. A realistic estimate of timing across PLLs along with an integrated place and route environment makes Precision RTL a powerful synthesis solution for designing with newer devices like Stratix and Cyclone.

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