W H I T E P A P E R

Achieving Design Closure with Constraint-Driven Synthesis

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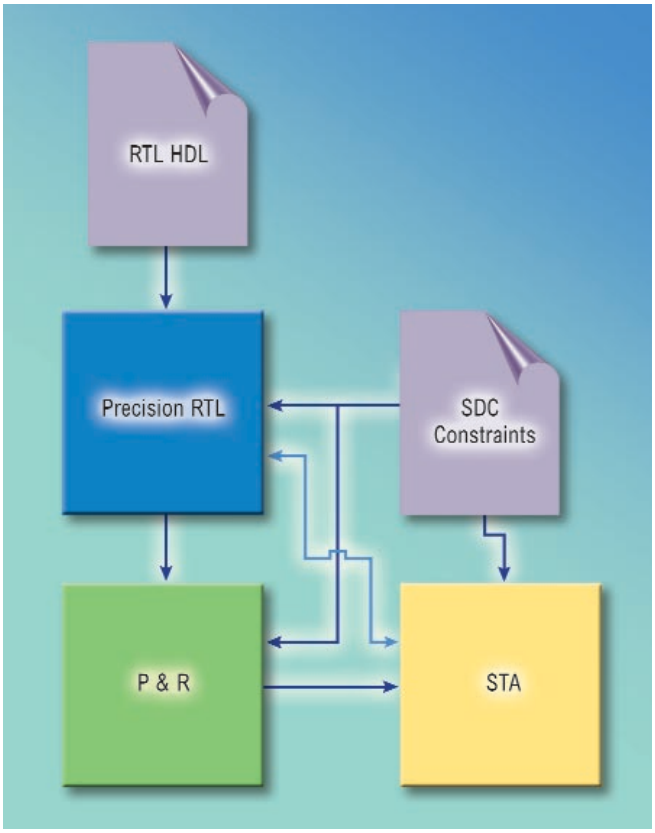
Constraining FPGA Designs

As the use of Field Programmable Gate Arrays (FPGAs) continues to become the hardware design engineer's choice for implementing custom logic and Intellectual Property (IP), there is an ever-developing need for the EDA industry to standardize on a common constraint language. This will not only ensure interoperability between FPGA synthesis and place-and-route tools, but will allow accurate description of "designer intent" to achieve design closure. Synopsys® Design Constraint (SDC) format has become the industry de facto standard for ASIC designers to communicate "design intent" to drive synthesis, Static Timing Analysis (STA), placement and verification (Figure 1). With FPGAs now replacing ASICs for many applications, SDC is becoming the obvious choice for an FPGA design constraint language.

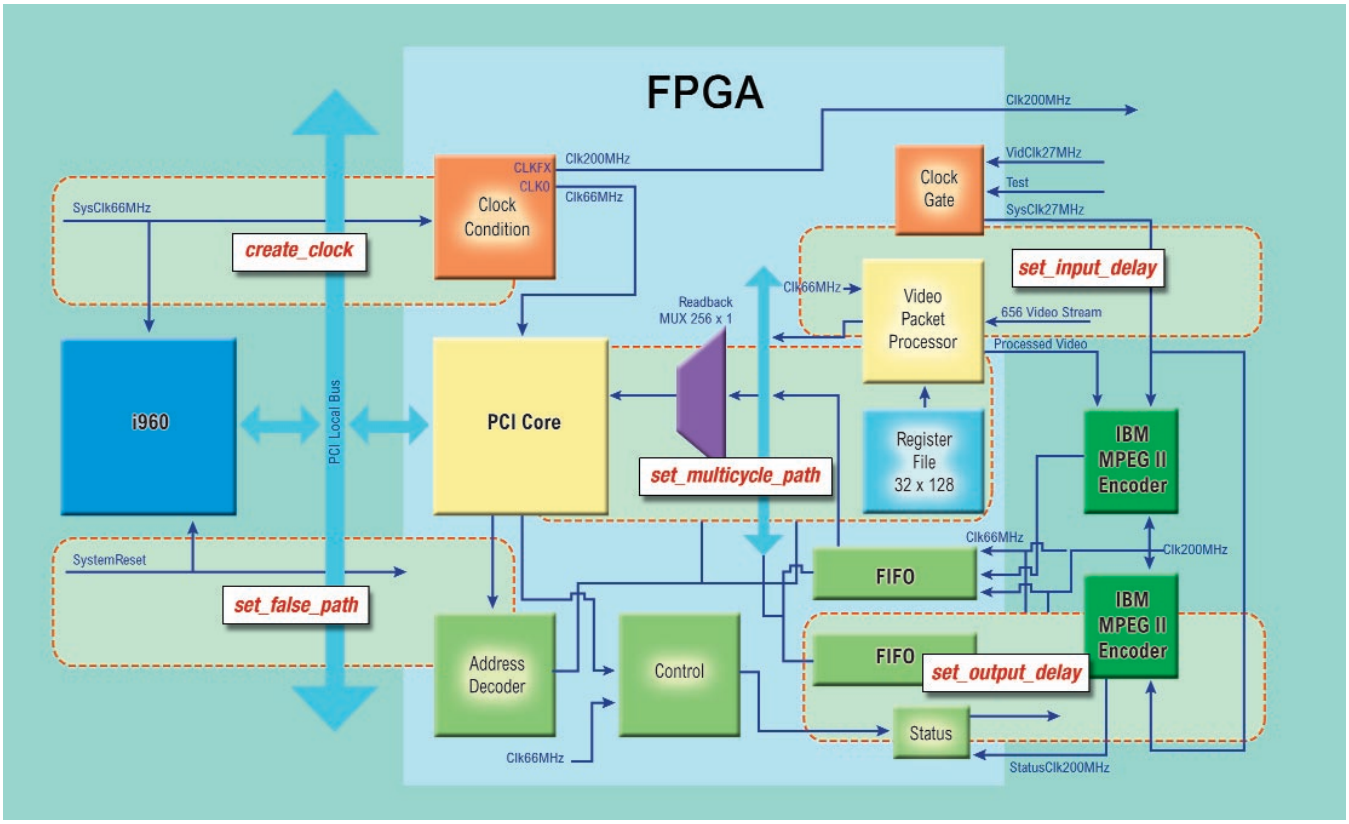
With the advent of constraint-driven synthesis and place-and-route tools, the importance of accurately describing design performance and implementation requirements through the application of design constraints has risen dramatically. These tools employ user-defined design requirements in the form of design constraints and attempt to achieve design closure. An improperly or insufficiently constrained design can lead to long run times, multiple design iterations and/or sub-optimal results.

In the past, it was sufficient to constrain a design based solely on operating frequency (Fmax) requirements, and perhaps some additional I/O constraints (typically expressed as internal chip setup and clock-to-out times). However, this type of constraint methodology did not consider board-level timing requirements or chip-level timing paths whose requirements were not as stringent as the Fmax constraint. To compensate, a complex method was used to calculate setup and clock-to-out constraints, based on desired Fmax, board delay, uncertainty and the AC characteristics of the other components within the system. Worse yet, these calculations had to be re-done any time the Fmax was changed.



SDC has become the most widely adopted and documented constraint language in the EDA industry, largely because it facilitates the communication of design requirements between EDA tools. SDC is a command language based on the

EDA industry-standard Tcl syntax and provides the ability to fully constrain a design for timing (Figure 2). The commands are generally grouped between timing constraints, timing exceptions, environment commands and object commands. The timing constraints and timing exceptions commands *create_clock* , *set_multicycle_path* and *set_false_path* play a vital role in fully describing "design intent." The *create_clock* command defines the system operating frequency while *set_false_path* or *set_multicycle_path* defines timing exceptions or relaxes the operating frequency.



Unlike the traditional FPGA constraint languages used in many legacy synthesis tools, SDC enables designers to constrain the chip's I/Os based on the timing behavior of the off-chip logic and PCB interconnect delay. Because it is usually dominated by the off-the-shelf parts that populate the board, off-chip logic timing is typically fixed. By constraining the I/Os based on the specified timing of the off-the-shelf parts, board-level timing is satisfied when the design passes synthesis and place-and-route timing analysis. No additional analysis against board-level requirements is needed in most cases.

SDC also enables the designer to provide timing exceptions on selected portions of the design. Constraint-driven synthesis and place-and-route focuses on those design paths that violate the design constraints. Constraint-driven optimization algorithms will work harder to fix these timing violations by performing additional optimizations, inserting additional circuitry or trying additional placements. Timing paths that meet timing but are erroneously seen as violations can result in inefficient synthesis, longer runtimes and failure to place-and-route the design. These types of timing violations fall into one of two categories; false paths and multi-cycle paths.

False paths can occur for a variety of reasons and are of no concern to the designer. The designer can create a false path for a circuit that will not occur in normal operation. A path may be false because it's known that the circuitry involved will operate slower than the constraints indicate. Paths from master reset signals are often false since they can occur over many clock cycles — sometimes on the order of hundreds of milliseconds. There is no need to optimize this type of reset so it can operate at the FPGA clock frequency.

Multi-cycle paths are timing paths that are of concern to the designer. Multi-cycle path constraints can be relaxed by an integer multiple of clock cycles. An example would be a microprocessor interface with a wait-state. The wait-state indicates that the microprocessor needs an extra clock cycle for data to be transferred. Thus there is no need for the interface to transfer data in a single clock cycle and the timing constraints can be relaxed by using a multi-cycle path constraint.

The use of SDC as a common constraint language for FPGA design facilitates interoperability between synthesis and place-and-route tools and allows designers to accurately constrain their designs to take advantage of constraint-driven synthesis tools. SDC has the added benefit of being widely used by the EDA community — in effect, it has become the industry standard.

With today's larger and faster FPGAs, primitive constraints can no longer meet designers' needs. Next generation tools like Mentor Graphics Precision™ Synthesis have been designed to take advantage of advanced timing constraints. With many of the FPGA vendors' place-and-route tools now migrating to SDC as well, designers will be assured interoperability between synthesis and place-and-route tools — facilitating accurately constrained designs that result in fewer design iterations and faster time-to-working-silicon.

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