Single-Chip System Manager

Today's current system management implementations can require hundreds of discrete components. These solutions are often a collection of fixed function chips and discrete components that must work in concert to create a cohesive solution. Actel's flexible, single-chip, mixed-signal Fusion Programmable System Chip (PSC) can perform a host of system management tasks while replacing hundreds of chips.

Just one Fusion device can replace a CPLD, a real-time clock, a power sequencer, a temperature monitor, a fan controller, nonvolatile memory, clock generators and configuration memory.

While standards such as the Micro Telecom Computing Architecture (MicroTCA), AdvancedTCA and Intelligent Platform Management Interface (IPMI) are now being adopted, many of today's

implementations are proprietary, having evolved over time within an organization.

Driven by the need to increase system up-time and reliability, many designers are adding system diagnostics and prognostics, not only to help debug systems that have failed but also to identify potential failures before they arise.

Fusion integrates all the System Management Functions into a single-chip solution reducing board cost and complexity and improving reliability.

Turn to page 2 to find out how Actel not only provides a Ready-to-use device for System Management, but also a development platform, MicroTCA reference designs and easy to use software to deliver the complete standard or custom System Management solution.

System Management Functions

- Power Initialization
- Power Sequencing
- Reset Management
- Voltage Monitoring
- System Clocking
- Data Logging
- Remote Communications

- Diagnostics and Prognostics
- Errors and Alarms
- Current Monitoring
- SRAM FPGA Management
- Thermal Management
- MCU Boot Loader
- ID and Authentication

Actel News

Jan 30, 2007 Actel Expands Sales Channel in Greater China

Jan 29, 2007 Actel Champions Embedded Systems Designers with Broad Range of Industry-Standard Processor Solutions

Jan 22, 2007 Mouser Electronics and Actel Corporation Enter Into Global Distribution Agreement

Jan 15, 2007 Actel and Mentor Graphics® Expand Partnership

Jan 15, 2007 Actel Refines Libero IDE to Improve Design Flow for Low-Power IGLOO FPGAs and Mixed-Signal Fusion PSCs

*Your **HOT ideas** – our **COOL solutions***

Actel Corporation is the leader in single-chip FPGA solutions

ONE CHIP is all you need

John East » View Point

System management continues to gain importance in the design of electronic systems as reliability and uptime are key metrics by which OEMs can increasingly differentiate themselves. Smaller process geometries drive multi-volt devices and are more susceptible to voltage and temperature fluctuations. Boards must be able to initiate corrective action when fault conditions occur. As a result, designers and system engineers continue to search for system management solutions that reduce system cost while also improving reliability.

We believe there will be a dramatic acceleration in the adoption of highly flexible and integrated solutions, such as our Fusion mixed-signal FPGAs, in lieu of utilizing hundreds of discrete components for system management.

Actel also offers designers several solutions beyond silicon – from MicroTCA reference designs to a system management development kit – to remove "the pain" associated with system management and decrease cost and risk.

Moving forward, we will continue to offer comprehensive solutions to our customers to ease the burden associated with the design of today's complex systems.

John East
CEO, Actel Corporation

On-Demand System Management and MicroTCA Webcast

Describes how Fusion can be used to integrate system management and Actel's commitment to deliver free MicroTCA reference designs.

Integrated System Management

Actel, the world leader of mixed-signal FPGAs, now offers the only single-chip system management solution. The Actel Fusion Programmable System Chip (PSC) integrates configurable analog, large Flash memory blocks, comprehensive clock generation, and high performance programmable logic in a monolithic device.

Fusion does not require additional configuration nonvolatile memory in order to load the device configuration data at every system power-up, which reduces cost and increases security and system reliability. Increased Fusion functionality can remove several additional components from the board, such as Flash memory, discrete analog ICs, clock sources, EEPROM, and real-time clocks, thereby reducing system cost and board space requirements.

For System Management visit : actel.com/products/solutions/systemmgt/

# System Management Developer's Kit
With Sample Designs

Actel's Fusion-based kit provides an excellent platform for developing system management applications and/or microprocessor applications. The kit includes an ARM-enabled Fusion device, a system management GUI, and sample designs to speed development and understanding of Fusions capabilities.

The system management GUI displays board status, application data, IPMI data and a graphical display of analog data.

The GUI helps users to:

• Monitor power supplies • Monitor temperature sensors • Set LEDs and text for display
• Set and read the RTC • Display embedded Flash contents

For Kit info visit : actel.com/products/hardware/devkits_boards/systemmgt.aspx
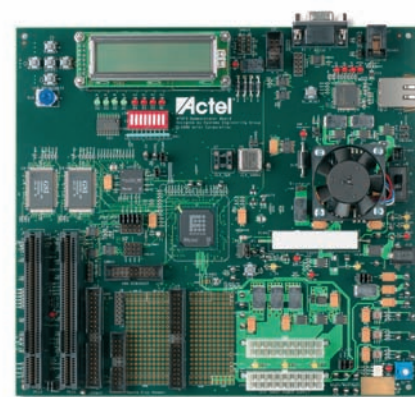
Libero IDE v7.3

Libero IDE v7.3 released in January provides new easy-to-use features that will aid designers utilizing the mixed-signal Actel Fusion PSC. "SynaptiCAD™'s WaveFormer Lite™ v1.1 allows Actel Fusion users to quickly generate analog waveforms by choosing a waveform equation and its parameters," said Dan Notestein, president and CEO of SynaptiCAD.

Get your Free Libero Download at : actel.com/products/software/libero/

ONE CHIP
is all you need
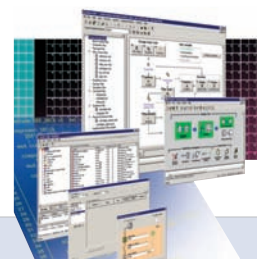
Simplify MicroTCA Design
and Lower Costs with the World's First Mixed-Signal FPGA

Actel's MicroTCA free and open reference designs drastically reduce risk, component count, and time to market. Actel uses the Fusion Programmable System Chip to implement MicroTCA solutions. MicroTCA (Micro Telecommunications Computing Architecture) is a standard that reduces the cost of telecommunications, industrial, medical, and military equipment.

Similar to replacement of the mini-computer by the personal computer, a variety of electronic equipment can be replaced by a modular, high availability, low cost MicroTCA chassis.

Actel provides highly integrated solutions for MicroTCA system management. Actel supports the Fusion-based solutions with reference designs, semiconductor intellectual property (IP), software, and customization services that enable quicker time to market for Actel customers with reduced risk, lower costs, and improved availability over existing solutions. The high integration of Actel MicroTCA solutions also provides increased functionality in a fixed form factor.

Actel Solutions for MicroTCA

- Power Module (PM) - **NOW**
- Advanced Mezzanine Card (AMC) – **NOW**
- MicroTCA Carrier Hub (MCH)
- Cooling Module (CM)
- Power Supply

Actel reference designs are tested at the MicroTCA interoperability workshops to ensure compatibility with the standard as well as with a variety of MicroTCA systems.
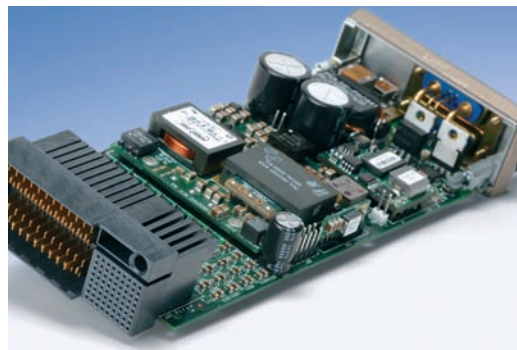
μTCA President Mike Franco μTCA™

"MicroTCA is poised to capture large shares in markets which need low-cost, high-reliability, remotely-managed systems. I am pleased to see Actel's commitment to support the MicroTCA design community with Fusion and several comprehensive reference designs. An early semiconductor entrant, Actel is well positioned to capture a significant share of this promising market."

Mike Franco
president, CEO, and chairman of the MicroTCA subcommittee.

MicroBlade delivers production-volume modules for MicroTCA applications.

Signal Stream Technologies offers support and customization of hardware and software design.

FREE Fusion-Based Reference Designs

MicroTCA Power Module (PM)

Actel has introduced a Fusion-based MicroTCA PM reference design that meets the MicroTCA specification version 1.0 and includes an enhanced module management interface (EMMC). Core8051 and two CoreI2C cores are the foundation for an IP and software platform that includes an IPMI protocol stack per IPMI specification 2.0, which supports the IPMB-0 connection and the power module EMMC interface to the MicroTCA carrier hub. **This is the first free and open reference design available for MicroTCA.**
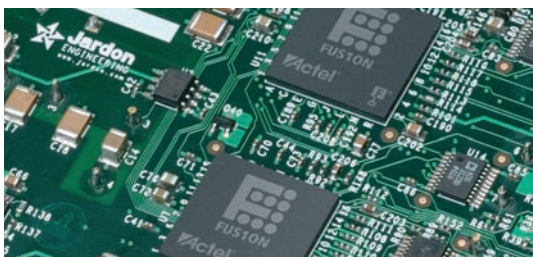
Advanced Mezzanine Card (AMC)

As in the Power Module reference design, Actel has reduced the part count required for the Fusion-based MicroTCA mezzanine card in a unique reference design platform that includes hardware, software, and intellectual property. The reference design is ready to plug in for evaluation and interoperability testing and conforms to the PICMG® AMC.0 ECR001 RC1.0 specification. It includes a module management controller (MMC) based on Core8051 and CoreI2C with 8051 application code.
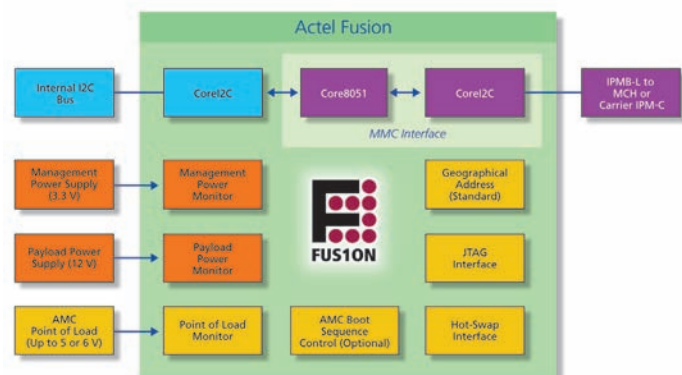
Industry Standard AMBA Peripherals *AMBA*

ARM and AMBA Processors

CoreABC, **Core8051s** and **CoreMP7**, Actel's soft IP ARM7 processor, all connect to the AMBA bus.

The following list of cores, supplied by Actel can be used with this bus and therefore any of these processors:

- » Core10/100
- » Core429
- » CoreAHB2APB
- » CoreAI
- » CoreCFI
- » CoreFMEE
- » CoreFROM
- » CoreI2C
- » CoreInterrupt
- » CoreMemCtrl
- » CorePWM
- » CoreSMBus
- » CoreTimer
- » CoreUART_APB
- » CoreWatchdog
- » Any user defined core compatible with AMBA bus prototcols

These cores and processors are all available within CoreConsole.

For FREE download visit:
actel.com/products/software/ coreconsole/

For embedded systems designers, Actel offers a broad range of industry-standard microprocessors.

Because there is an abundance of third-party software and support available for industry-standard architectures, Actel's portfolio allows designers to use the processors and tools they are familiar with when using Actel's innovative FPGAs. This broad portfolio enables designers to select the best processor for their application and easily combine it with the core benefits offered by Actel's Flash-based FPGAs – ease of design, reprogrammability, and reduced development cost and risk.

Recently, Actel added two new controller cores -- the small, easy-to-use CoreABC and the

configurable Core8051s – to its processor library. Like all Actel processors, these new cores operate with the industry-standard AMBA bus interface, enabling flexible, cost-effective system-on-chip (SoC) solutions across a broad range of markets and applications. Worldwide support for the AMBA bus enables designers to find and implement the specific functional elements needed for their embedded designs.

CoreABC is a powerful and easy-to-use solution for a broad range of embedded control applications. It is also the industry's smallest and first RTL programmable soft micro for FPGAs.

Core8051s is a configurable version of Actel's popular Core8051. The controller features one clock per instruction throughput and supports a range of configurable peripheral functions. Core8051s connects to the APB bus for easy integration with other APB peripherals using Actel's CoreConsole tool.
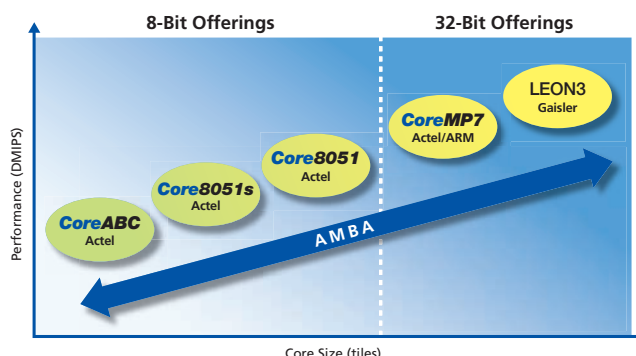
*Soft*Console *– Free µP Development Environment*

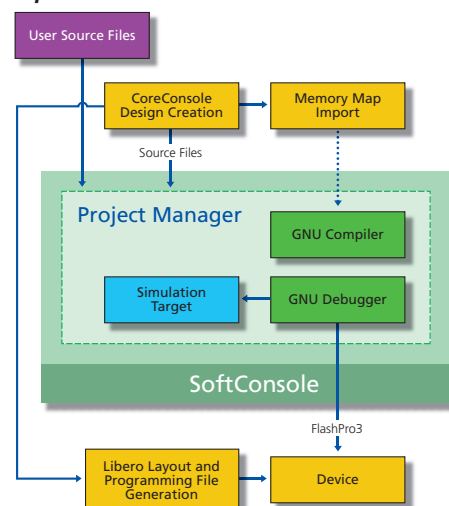*Soft*Console **available for FREE download and use with Actel FPGA optimized processors**

SoftConsole Includes:

» SoftConsole Eclipse-based IDE

» GNU C Compiler

» GNU Debugger GDB

» FREE basic debug support for CoreMP7

» Support for programming and debug with FlashPro3

SoftConsole is a free software development environment, including free compiler and debugger, enabling the rapid production of C and C++ executables for Actel Processors.

SoftConsole graphical user interface manages your software development projects. The GNU C/C++ compiler lets you write software that is immediately compiled into usable binary code.

SoftConsole includes a fully integrated debugger that offers easy access to memory contents, registers, and single-instruction execution. Programs developed with SoftConsole can be debugged on a target board or in the tool's simulator using the same uniform interface.

SoftConsole seamlessly integrates with CoreConsole for IP delivery and stiching to accelerate project completion and time to market.

For FREE download visit : actel.com/download/software/softconsole/

CoreABC – programmable soft Micro

CoreABC is a powerful and easy to use solution for a broad range of embedded control applications. It is also the industry's smallest and first RTL-programmable soft micro for FPGAs.

CoreABC features deterministic operation, very fast I/O response (less than 100 nanoseconds) and supports the advanced peripheral bus (APB) interface. Since CoreABC can be implemented in as few as 241 tiles, it can be used in small Actel devices, such as the Flash-based A3P030 ProASIC3 device. Implementation for CoreABC starts at less than 10 cents per instantiation.

CoreABC can be used on the following Actel devices:

- **Fusion**
- **ProASIC3/E**
- **ProASIC^PLUS**
- **Axcelerator**
- **RTAX-S**

CoreABC is delivered through CoreConsole and includes:

- **Free obfuscated version**
- **RTL version available for $5,000**
- **Test benches – VHDL & Verilog**
- **Core documentation**

CoreABC can be programmed in either hardware or software. The instructions executed are either held in a small internal ROM constructed from logic tiles (hardware programmed), or stored in RAM blocks internal to CoreABC (software programmed).

The RAM blocks can be initialized using the embedded Flash memory within the Fusion family or another external source (e.g., CoreMP7).

CoreABC stands for APB Bus Controller.

CoreConsole

The CoreConsole IP Deployment Platform (IDP) simplifies construction of a processor subsystem and assembly of IP blocks within a design.

CoreConsole Features:

- » Enables rapid assembly of system-level designs
- » IP deployment platform with secure IP vault
- » Supports IP block stitching and configuration
- » Intuitive, easy to use graphical user interface (GUI)
- » RTL output seamlessly passed to Libero IDE
- » Automatic system testbench generation
- » Includes configurable processor subsystem blocks
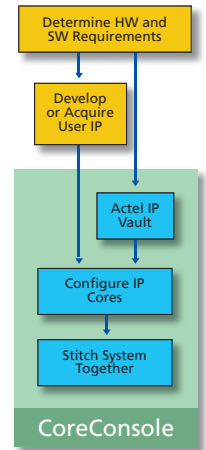
Now available for FREE download and use with Actel FPGA optimized processors.

For Free Download visit : actel.com/products/software/coreconsole/

CoreABC architecture
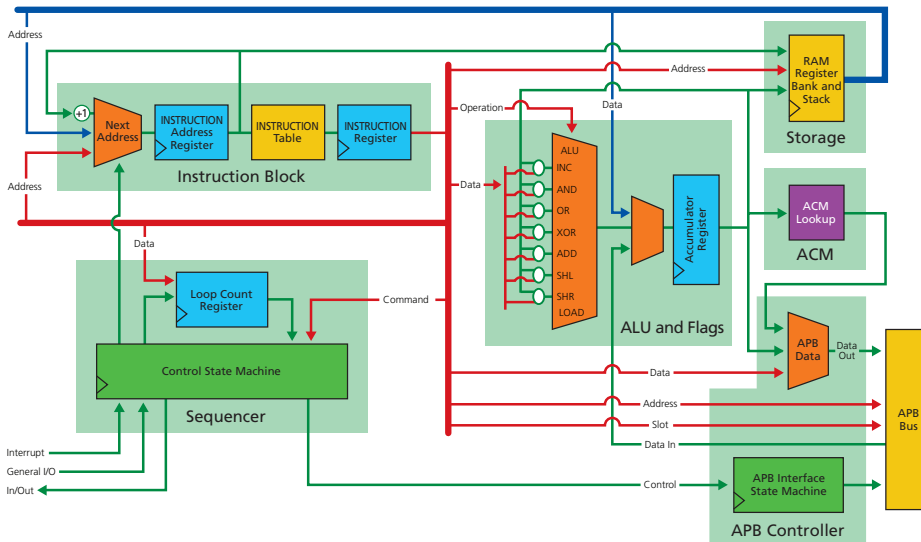
| Instruction Block	Contains instruction counter and instruction table and instruction to be executed
ALU and Flags	Each supported ALU operation can be disabled to reduce size
Storage	Provides local storage for data values and the call stack
ACM Lookup	Small lookup table that holds CoreAI initialization data
Sequencer	Controls operation of the core and handles interrupts
APB Controller	Implements the APB bus protocol and data input MUX

CoreABC

Fusion Design Example

A CoreABC-based system that can monitor analog inputs, adjust output levels, and report status via an RS-232 link using CoreUART can be implemented in an AFS090 device leaving 60% of device logic for other user functions. CoreAI is the Analog Interface core that allows a processor to easily control the Analog portion of the Fusion device. CorePWM (Pulse Width Modulation) generates up to 8 general purpose PWM signals.

Tile counts for this example:

CoreABC	241	APB Bus	125
CoreAI	150	CorePWM	87
CoreUART	300		
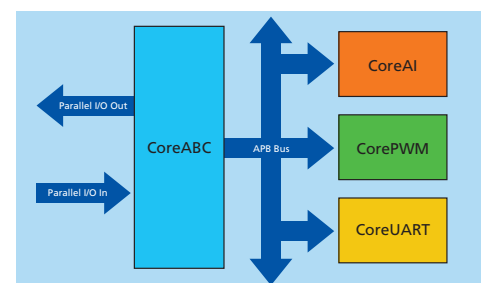
Motor Control Kit

Ishnatek, Actel's partner, has created a reference system using a Fusion Starter Kit to illustrate the Fusion Motor Control application.

The solution includes the board and a reference design so that you can run a stepper motor or a Brushless DC Motor (BLDC).

The software GUI helps you control the stepper motor or the BLDC motor in its different modes.

For Kit Info visit:
actel.com/products/solutions/ motorcontrol/ref_design.aspx

Closed Loop Motor Control

The Actel Fusion mixed-signal FPGA offers unprecedented integration by combining mixed-signal analog, Flash memory, and FPGA fabric in a monolithic Programmable System Chip (PSC).

For the first time, engineers can combine the motor control analog front-end, high speed Flash lookup tables, and deterministic algorithm processing capabilities of programmable logic in a single-chip solution.
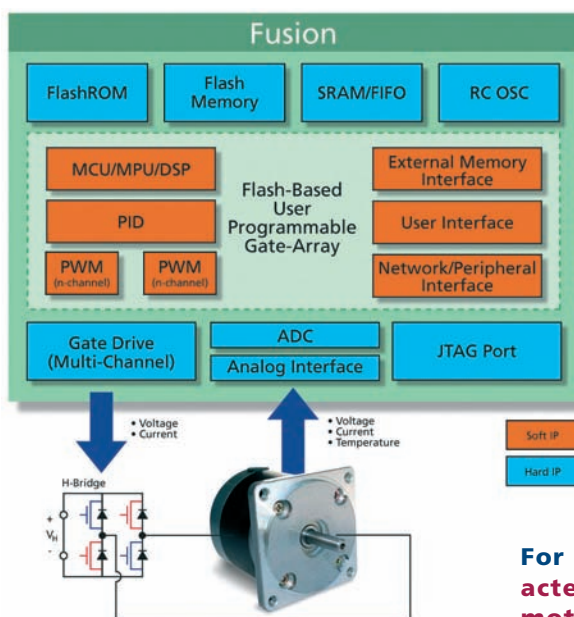
Fusion Motor Control Advantages

Single-chip solution

- Increased reliability, smaller form factor and board space

Functional integration

- System Manager and motor control in a single chip
- Data logging and subsystem diagnostic
- Can support multiple motors simultaneously

Multiple types of analog data acquisition

- Direct sampling of voltage, current, and temperature

Single platform

- supports multiple standards for local and remote communications.

For Motor Control visit :
actel.com/products/solutions/ motorcontrol/
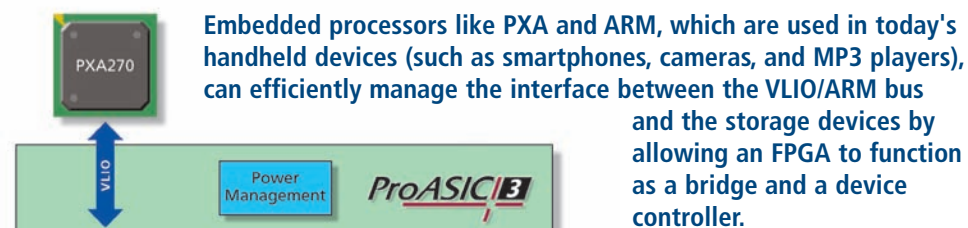
WINNER
FlashPro Lite 2000th unit

Actel awarded a Fusion Starter Kit to our 2000th customer of FlashPro Lite. FlashPro Lite is Actel's dedicated programmer for ProASIC^PLUS devices.

Mr. Tasuku Yuguchi, General Manager, R & D Group for Optex, receiving his Fusion Starter Kit

ProASIC3 Storage Solutions

Embedded processors like PXA and ARM, which are used in today's handheld devices (such as smartphones, cameras, and MP3 players), can efficiently manage the interface between the VLIO/ARM bus and the storage devices by allowing an FPGA to function as a bridge and a device controller.

The block diagram shows a ProASIC3 device interfacing with PXA270 and multiple storage interfaces like IDE ATA6, CE-ATA HDD, Secure Digital SD1.1/2.0 and MMC, CompactFlash 3.0, USB, and CardBus 2.1/PCMCIA.

The Storage Solution Board is provided through Actel's partner program.

Actel's RTAX-S Hits Major Reliability Milestone

Actel recently announced that its radiation-tolerant RTAX-S product family has successfully accumulated more than 1.4 million device-hours of life test data, which has yielded a failure in time (FIT) rate of 12.76.

A benchmark for the reliability of a product, one FIT is defined as one failure in 1 billion hours. Such a low FIT rate for a relatively new product is a huge testament to the reliability of the product.

During the course of reliability testing, 120 RTAX-S FPGAs each completed 6,000 hours of high-temperature operating life (HTOL) testing. Details of the reliability testing performed on the RTAX-S family can be found in the paper, "RTAX-S Testing Reliability Update," at http://www.actel.com/documents/RTAXS_Rel_Test_WP.pdf.

Designed to withstand the rigors of space-flight applications, the rad-tolerant Actel RTAX-S family offers unique features desirable for space-flight applications, including single-event upset (SEU)-hardened flip-flops with built-in triple module redundancy (TMR), 300 k bits usable error-corrected on-board memory and a large number of user I/O. The family also includes the 4-million gate RTAX4000S, the industry's largest space-optimized programmable logic device.
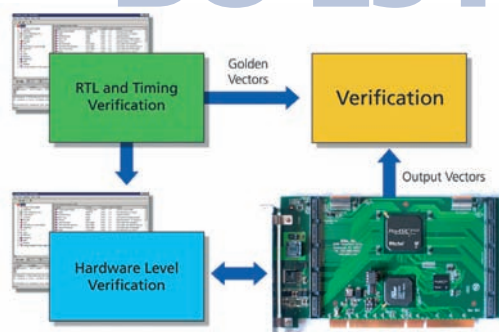
RTAX-S Prototyping

Commercial RTAX4000S

*Prototypes of the four million-gate RTAX4000S is available now.*

Using this, designers can obtain the same architecture, density, timing and packaging options offered by space flight-quality RTAX-S devices, without the added costs of MIL-STD 883 processing and hermetically sealed packaging. With the prototype, designers can validate a design and evaluate performance before programming a fully qualified FPGA, leading to significant reductions in overall design risk, time and costs.

Reprogrammable RTAX-S Prototyping

Allows Designers to use Flash-based FPGAs

The new Aldec/Actel RTAX-S prototyping solution allows aerospace customers to take advantage of Actel's Flash-based reprogrammable ProASIC3/E devices for flexible Flash-based prototypes.
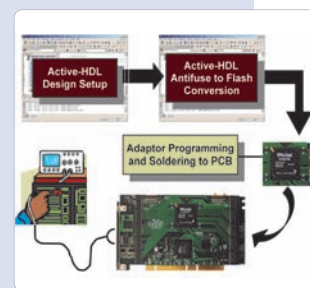
The use of this new tool allows rapid reconfiguration of development platforms for space-flight computing, permitting faster integration and co-development of hardware and software. As part of the solution, a prototyping adaptor is provided, which maps the footprint of Actel's ProASIC3/E device to the footprint of a radiation-tolerant RTAX-S device. Customers can therefore use the reprogrammable prototyping tool without altering the layout of their space-flight printed circuit board (PCB).

Available now, the complete prototyping solution includes an adaptor board, programming kits and the hardware and software tools needed for design conversion, mixed VHDL and Verilog simulation, mapping and programming. Pricing is dependent on the target space-optimized RTAX-S device and package.

DO-254 for Programmable Devices
Hardware/Software Verification Platform

DO-254

Adopted by the Federal Aviation Administration, the DO-254/EU80 (Design Assurance Guidance for Airborne Electronic Hardware) specification provides design assurance guidance for the development of "safe" airborne electronic hardware, including FPGA designs intended for flight use.

With the industry's first hardware/software verification package to ease DO-254 certification, Actel and Aldec are alleviating the verification bottleneck in the design assurance process. The hardware/software verification platform includes software tools to capture and compare simulation data with a golden set of vectors as well as a customized board for the functional verification phase of the DO-254 compliance process.

Actel's Protocol Design Services Group offers design and verification services and solutions for customers designing FPGA-based avionics applications that require DO-254 compliance. The Protocol DO-254 design and process flow expertise combined with the new Actel and Aldec verification platform could be instrumental in ensuring the flight-worthiness and safety of avionics designs.

ALDEC
The Design Verification Company

www.actel.com Makeover

Actel's recently launched new and improved website not only includes a clean crisp design, but a more robust architecture that allows users to easily navigate throughout the website to find up-to-date product information.

Brand-new capabilities include:

» Actel's Online Store, operated by Mouser Electronics

» Dedicated search engines for Press Releases, Knowledge base articles, Intellectual property cores and of course, the entire website

» RSS News Feeds, a free service that brings all the latest Actel news right to your desktop.

Visit Actel's new website today and see what the buzz is about.

Actel Live – Where you can find out how your **hot ideas** can work with our **cool solutions**

Upcoming Speaker Presentations

EVENT	DATE	SPEAKER	DETAILS
FPGA 2007	Feb 19, 2007 9:00 AM	Wenyi Feng Sinan Kaptanoglu	**Designing Efficient Input Interconnect Block for LUT Clusters Using Counting and Entropy** Monterey Beach Resort, Monterey, CA
FPGA 2007	Feb 19, 2007 2:00 PM	Kai Zhu	**Post-route LUT Output Polarity Selection for Timing Optimization** Monterey Beach Resort, Monterey, CA
Globalpress Electronics Summit 2007	Feb 26, 2007 11:00 AM	Dennis Kish	**Panel: "Can Anything Save the ASIC?"** Monterey Plaza Hotel, Monterey, CA
Semico Summit 2007	Mar 12, 2007 1:30 – 2:00 PM	John East	Camelback Inn, Phoenix, AZ

Trade Shows

EVENT	DATE	PARTICIPATION	LOCATION
Hardened Electronics and Radiation Technology	Mar 5-6, 2007	Exhibitor	Marriott Mission Valley San Diego, CA, USA
International IC China	Mar 5-6, 2007	Exhibitor Booth #2H02	Shenzhen Convention and Exhibition Center, Shenzhen, China
International IC China	Mar 13-14, 2007	Exhibitor Booth #4P37	Shanghai Mart Shanghai, China
CMSE	Mar 13-14, 2007	Exhibitor	Sheraton Gateway Hotel Los Angeles, CA, USA
ESC	Apr 3-5, 2007	Exhibitor Booth #632	McEnery Convention Center San Jose, CA, USA
NSREC	Jul 24-25, 2007	Exhibitor	Hilton Hawaiian Village Honolulu, HI, USA

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Register for Product Updates
Stay up-to-date with Actel's latest product documentation: **www.actel.com/updates**

Actel is a must see on your visit to ESC. From Fusion, an FPGA with Analog front end, to IGLOO, the lowest power 5 µW FPGA. Actel and ARM® turn your **hot ideas** into **cool solutions**. Come tell us your idea?

McEnery Convention Center
San Jose, CA, USA
April 3-5, 2007 Booth #632
www.actel.com/esc2007

Avnet-Memec in conjunction with Actel will be hosting several workshops:

Integrating an ARM7™ CPU soft core in an Actel FPGA
For hardware design engineers.

Learn how to integrate Actel's CoreMP7 soft ARM7 core in a mixed-signal FPGA design.

This 90-minute, hands-on session is an abbreviated version of Avnet's SpeedWay Design workshop that teaches you the end-to-end tool flow for designing an Actel FPGA with an embedded ARM7 soft core. Primarily intended for hardware designers, the workshop will use the Actel Libero® Integrated Design Environment (IDE) to create a hardware design; tailor the IP and processor blocks using SmartGen and CoreConsole; synthesize the design; create a testbench and simulate; and place and route, analyze timing and power, and program the FPGA on the target board.

Software development for ARM7 CPUs embedded in an FPGA
For software and hardware design engineers.

Learn the software development process for Actel FPGA designs that have an integrated soft core ARM7 CPU.

This 90-minute hands-on session is the software accompaniment to our FPGA design workshop using Actel's Fusion™ mixed-signal FPGA with an embedded ARM7 soft core. This workshop is for both software and hardware design engineers that develop software for embedded processors. We will leverage Actel's SoftConsole software development environment to create a system management application in C; compile using the GNU C/C++ compiler; and use the GDB debugger to explore memory, CPU registers, and step through executing code on the target hardware.

Your **HOT ideas** – our **COOL solutions**

ONE CHIP is all you need