Power Distribution Network Design for Stratix IV GX and Arria II GX FPGAs

Transceiver Portfolio Workshops 2009

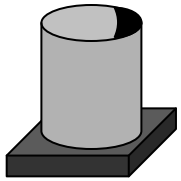
Question – What is Your PDN Design Methodology?

Easy

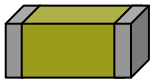
Complex

Historical

Full SPICE simulation

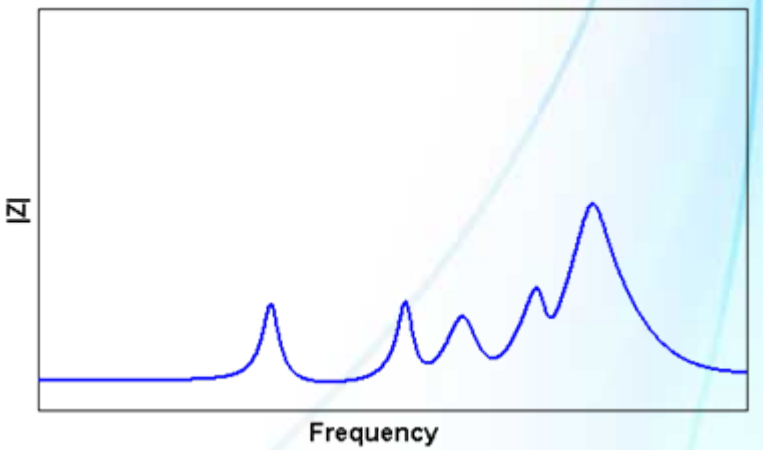


1 x 100µF cap



10 x 100nF cap

"I did it this way in all my previous designs"



Agenda

- Power integrity issues
- Challenges of 40-nm PDN design and Altera innovations to help
- What is the PDN?
- PDN design and decoupling schemes
- Power distribution network design
- Altera's PDN design tool flow
- Summary

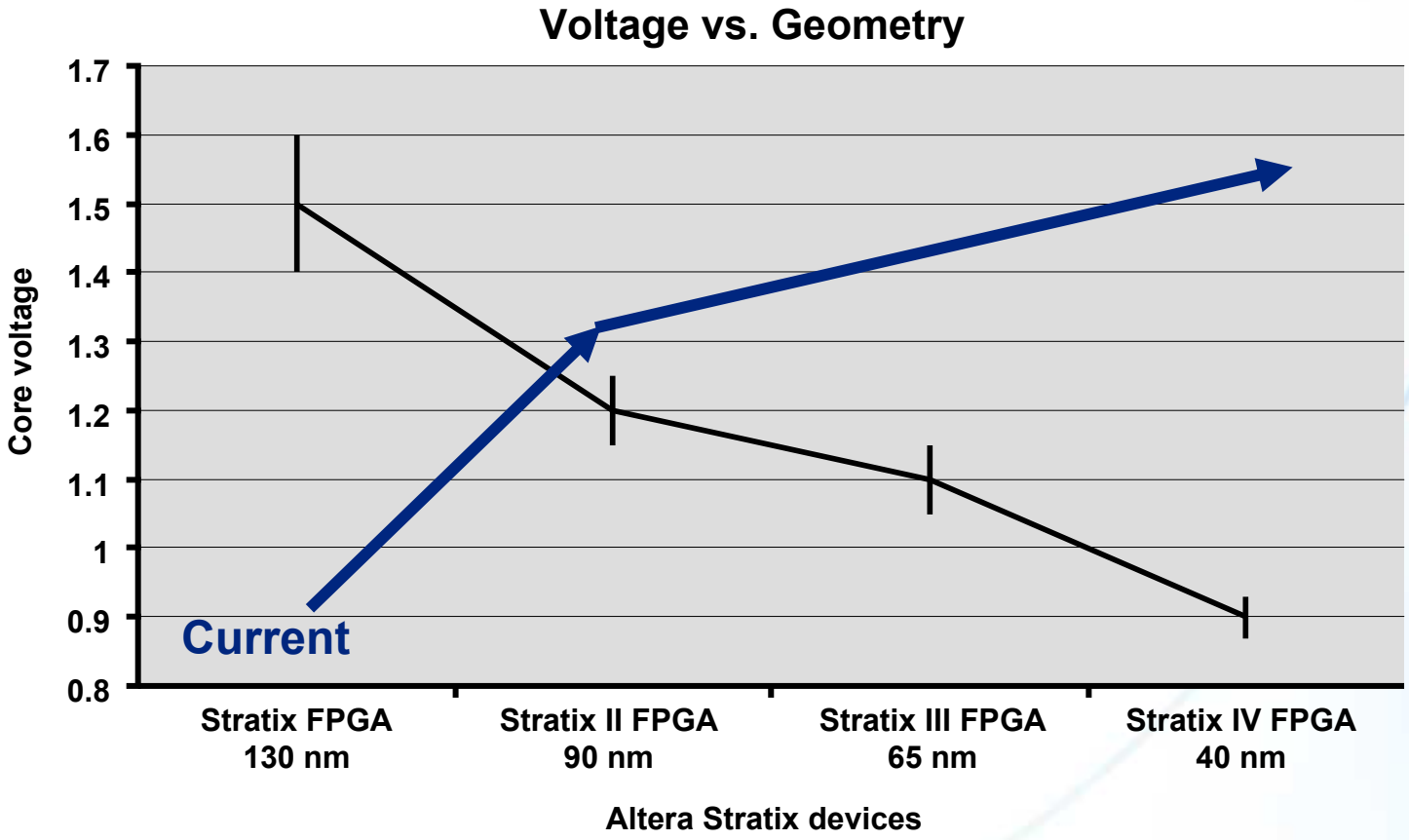
Common Power Integrity Issues

- Power integrity issues can result in:
  - Increased jitter
  - Poor timing results (decreased slew rate)
  - Device brown-out and metastability
  - Logic errors
  - EMI (electromagnetic interference) problems
- Power integrity issues can be:
  - Difficult to diagnose
  - Be found late in design cycle or post-deployment

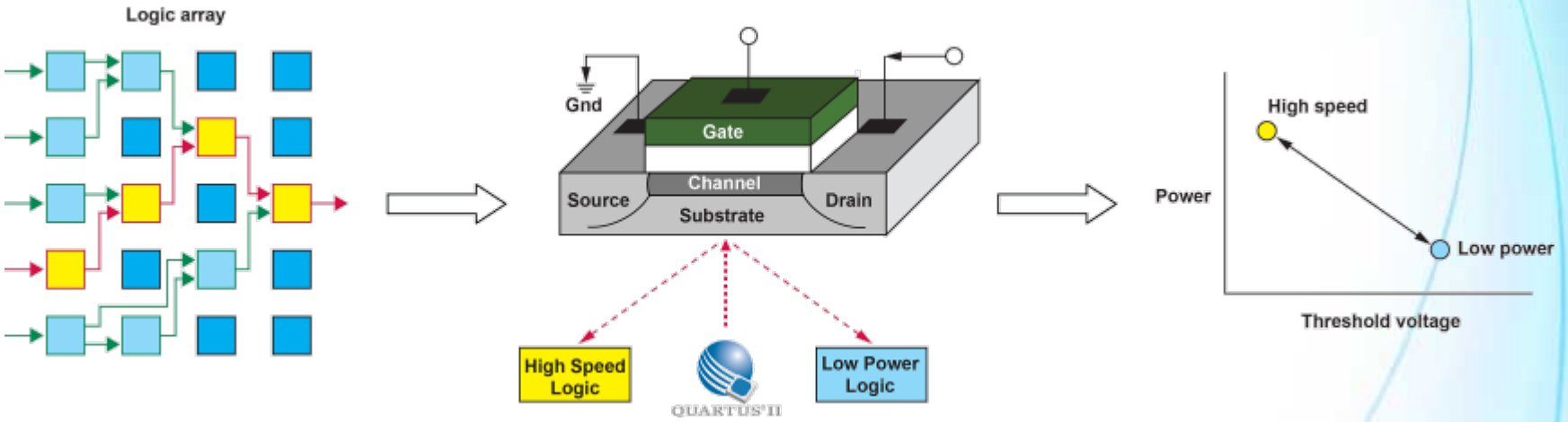
Need a power distribution network design methodology

Technology Challenges

- Larger densities and lower voltages with less noise margin create challenges for power design



Programmable Power Technology (PPT) for Stratix III and Stratix IV FPGAs

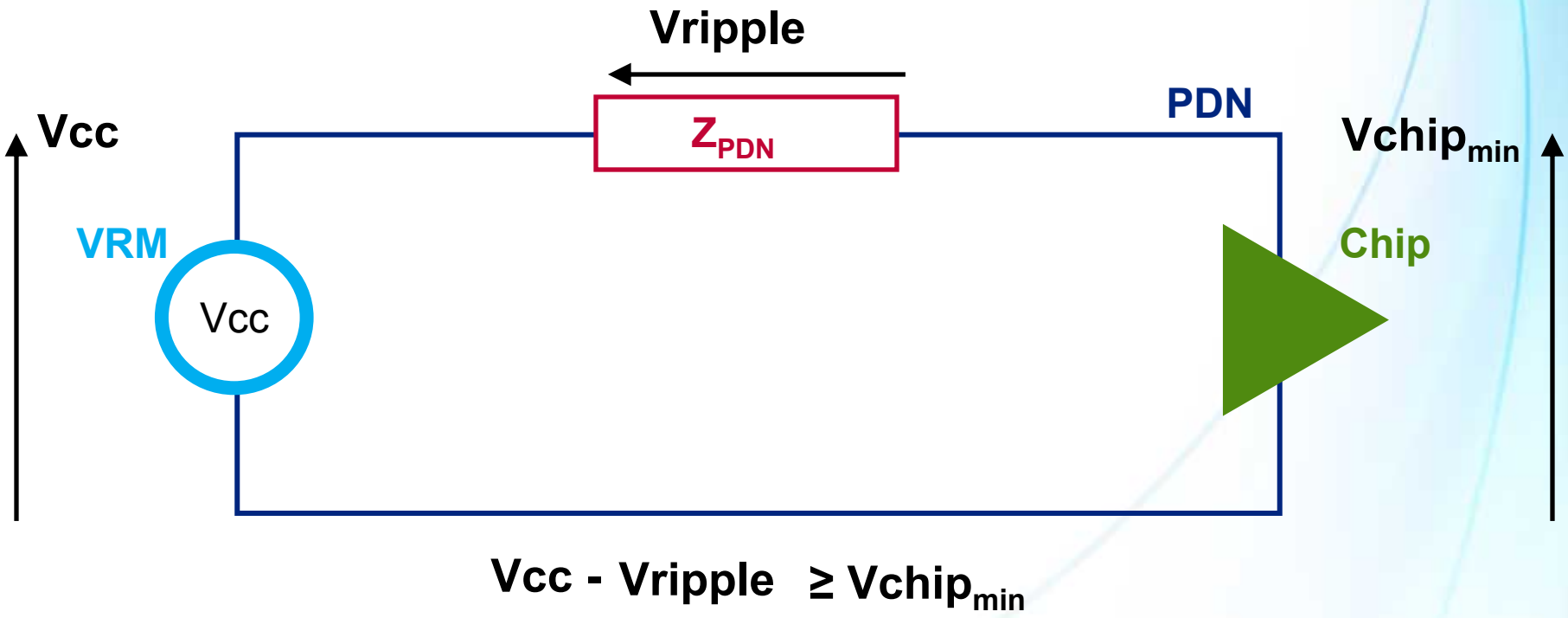


Quartus II software automatically adjusts transistor threshold voltage for low power and high performance

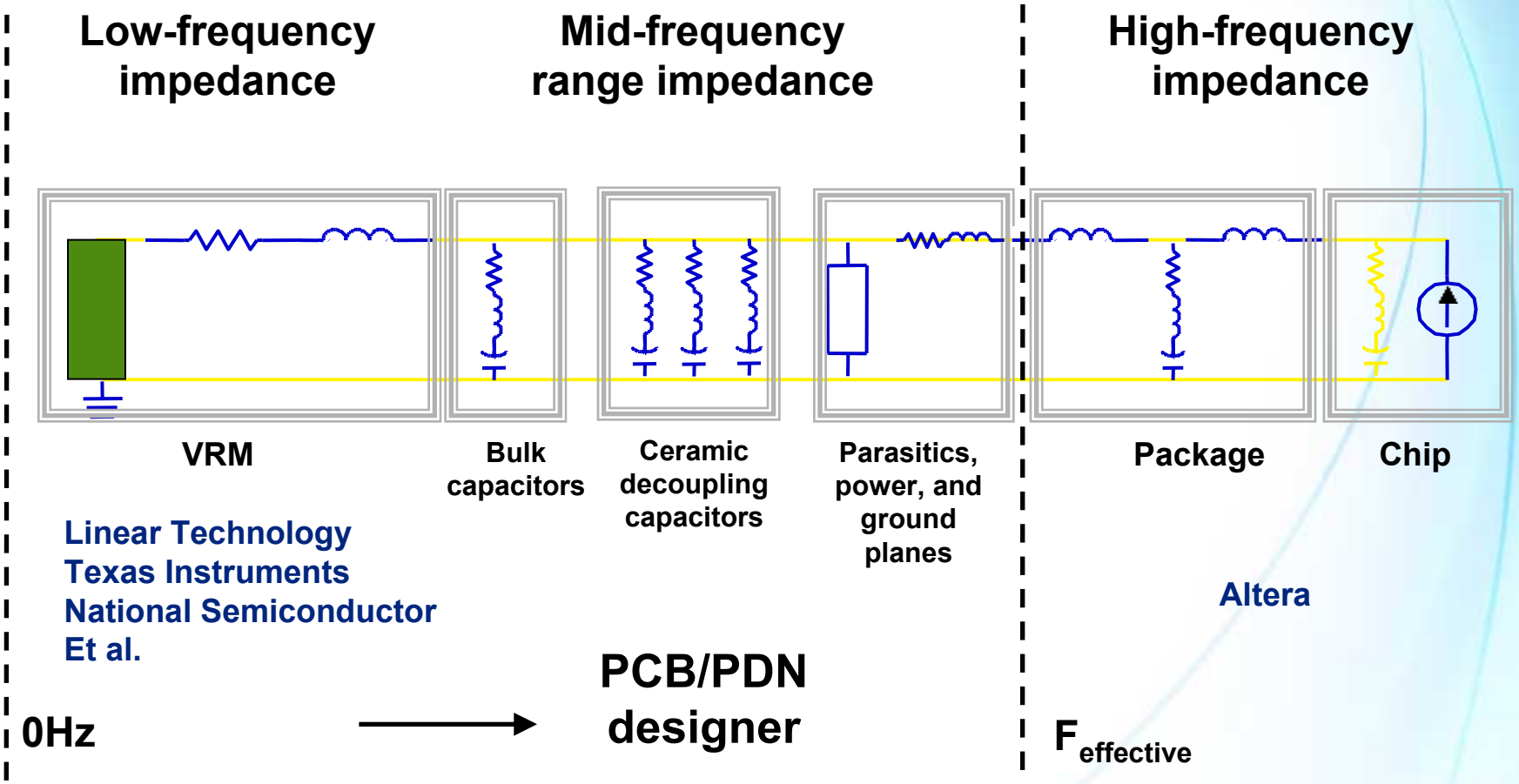
Note: A very simplistic "model" of Programmable Power Technology. Actual implementation varies and is patented.

Role of the PDN

- Distributes clean power to each device from the voltage regulating module (VRM) to the power rails of the chip
  - Keep ripple noise (rail collapse) < spec (typically 5%)
- Provides return path for I/O signals



Simplified Model of a PDN

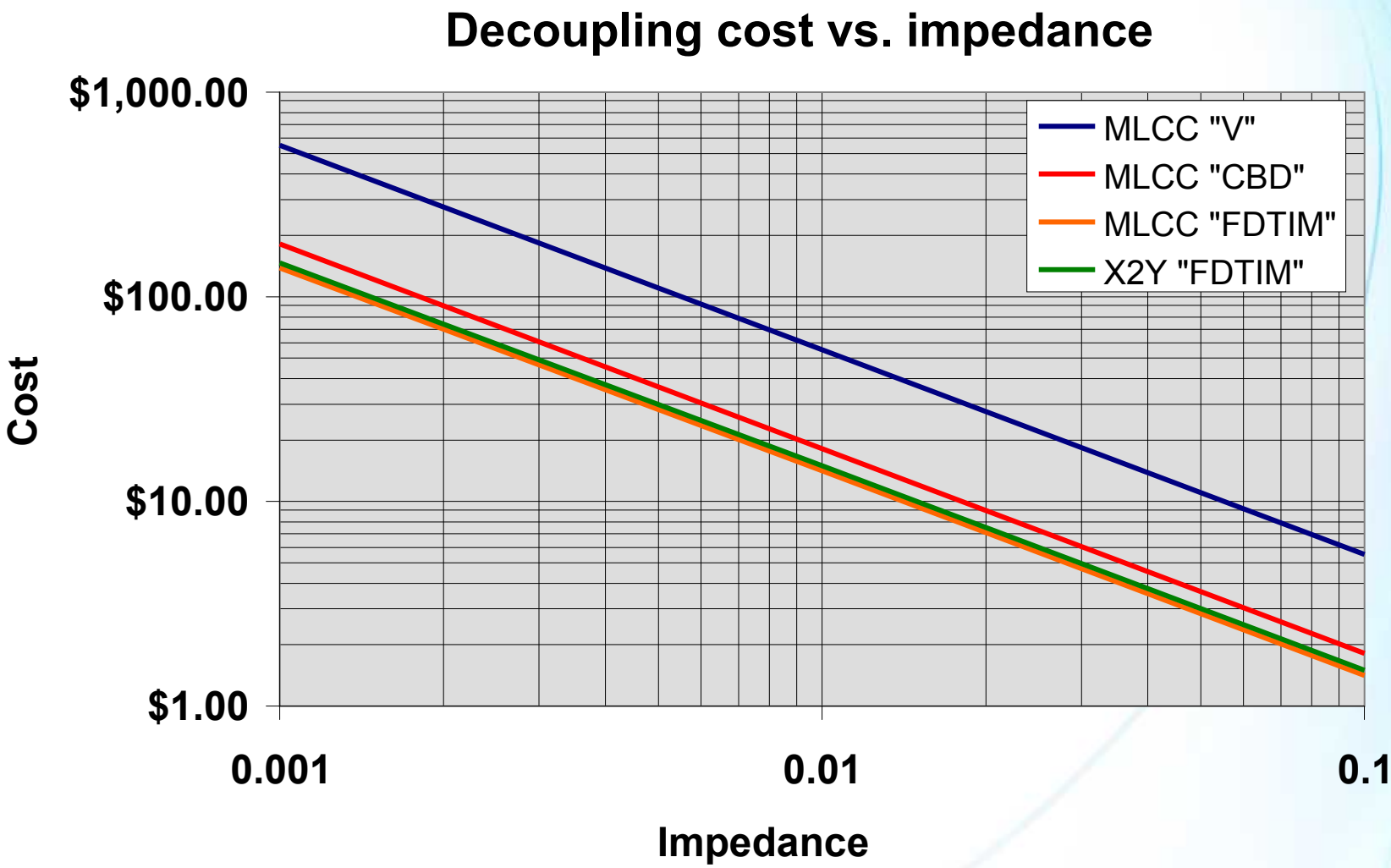


PDN and Decoupling Schemes

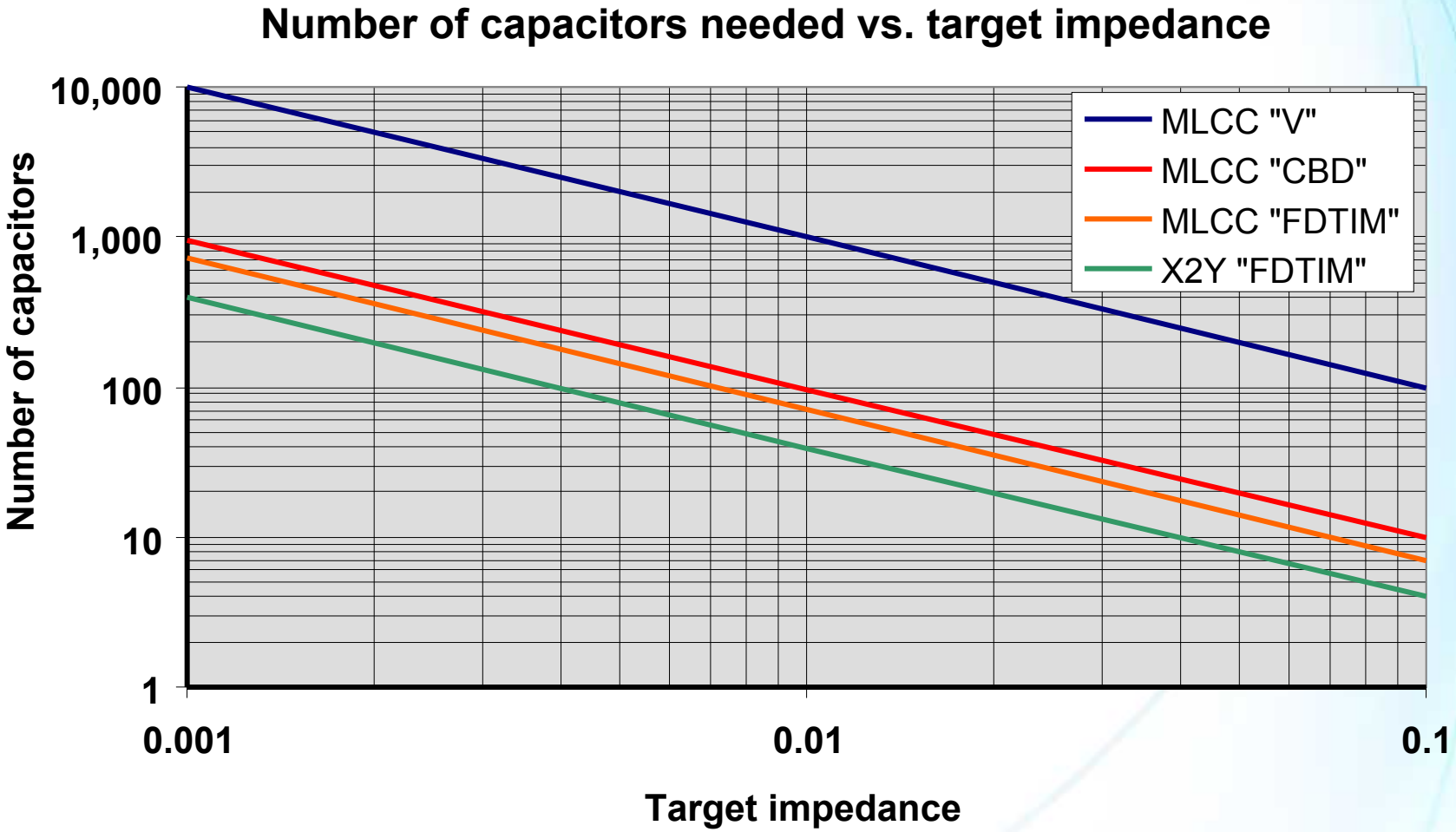
Different Schemes for Decoupling

- Frequency domain target impedance methodology (FDTIM) or multi-pole (MP)
  - Good: Least number of capacitors, very stable, and low cost
  - Bad: Requires analysis of the network and can require many different capacitor values
- Capacitors-by-the-decade (CBD)
  - Good: Less capacitor types than FDTIM and fewer capacitors than Big-V
  - Bad: Produces a more unstable solution than FTDIM with more capacitors, requires some analysis
- Big-V
  - Good: Least number of different capacitors, requires least amount of analysis
  - Bad: Requires the most amount of capacitors, making it inefficient, extremely costly, and possibly unstable
- Distributed matched bypassing (DMB)
  - Good: Most stable, requires less capacitors than Big-V or CBD
  - Bad: Requires the most analysis with costly embedded PCB resistors, capacitor value is locked per capacitor pad

Decoupling Cost for Each Scheme



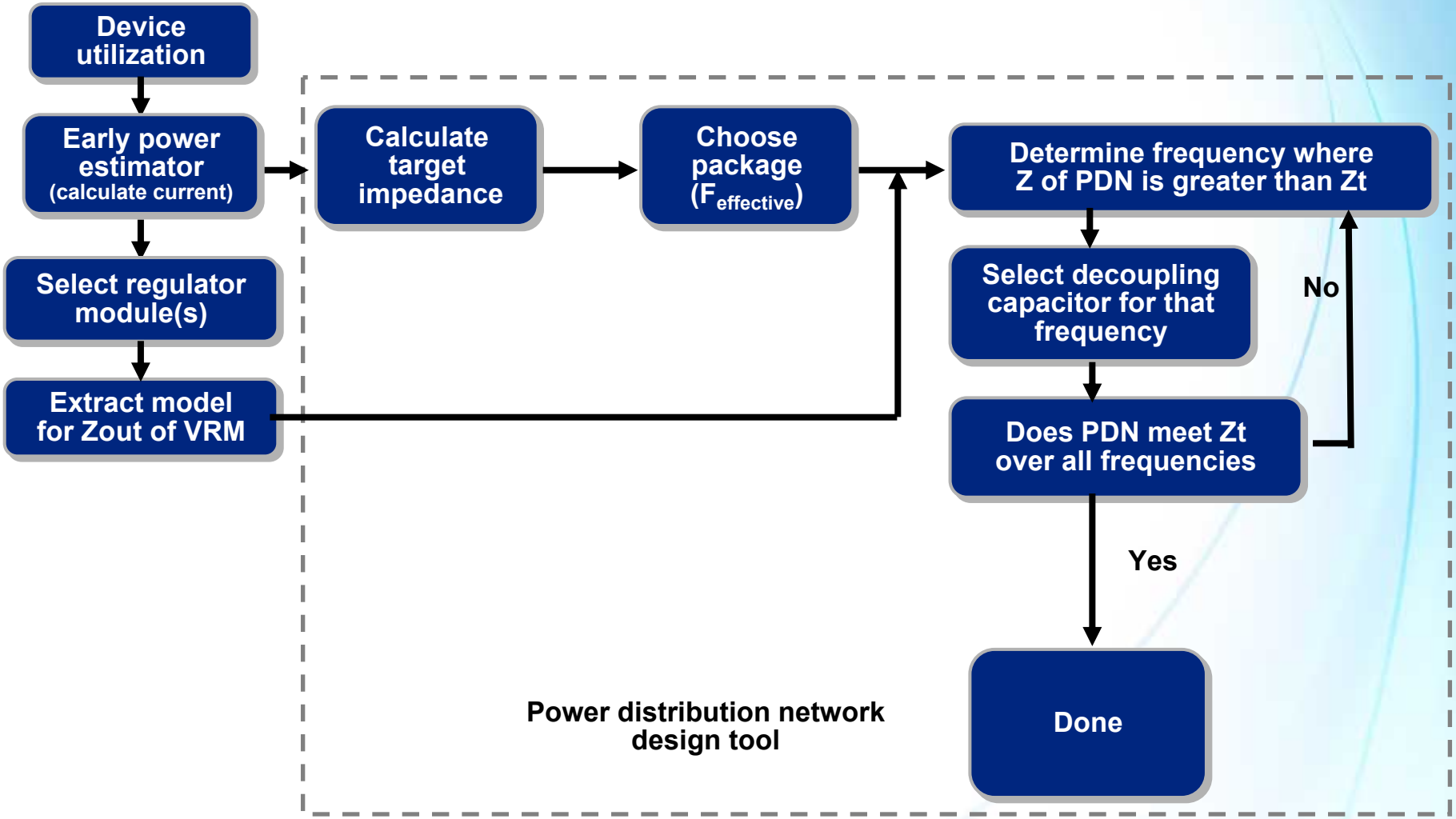
Capacitors Needed for Decoupling Scheme



Power Distribution Network Design

Altera's PDN Design Tool Flow

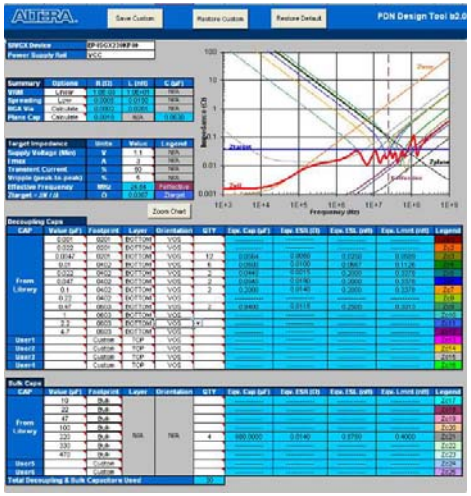
Power Distribution Network Design Flow

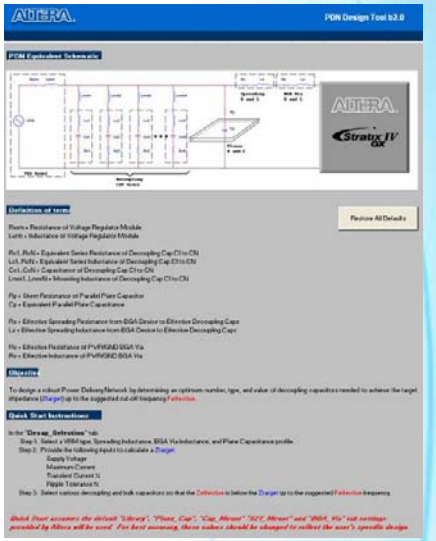


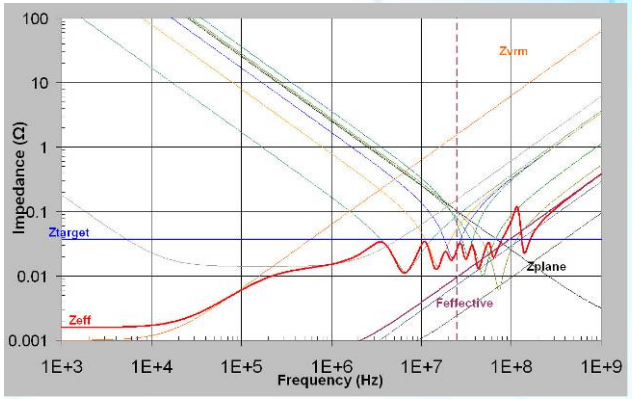
Altera's Power Distribution Network Design Tool

- Excel spreadsheet tool
- You supply:
  - Rail current
  - VRM choice
  - Package choice
  - PCB specification
    - Stack up, via size, capacitor outline
    - Spreading inductance
- You select:
  - Capacitor values and quantity
- Tool shows you:
  - Impedance plot over frequency

Robust, low-cost PDN suited to your design







PDN Design Tool Flow

Stratix IV GX FPGA – VCC supply example

SIVGX Device	EP4SGX230KF40
Power Supply Rail	VCC

Summary	Options	R (Ω)	L (nH)	C (µF)
VRM	Switcher	1.0E-03	2.0E+01	N/A
Spreading	Low	0.0005	0.0150	N/A
BGA Via	Calculate	0.0002	0.0261	N/A
Plane Cap	Calculate	0.0019	N/A	0.0630

Target Impedance	Units	Value	Legend
Supply Voltage (Min)	V	0.9	N/A
I max	A	3	N/A
Transient Current	%	50	N/A
Vripple (peak-to-peak)	%	3	N/A
Effective Frequency	MHz	24.84	Feffective
Ztarget = ΔV / ΔI	Ω	0.0180	Ztarget

- PDN tool setup
  - Select device (package)
    - With BGA, via and plane spreading generates $f_{effective}$
  - Select voltage regulator module (VRM)
    - Type
  - Select plane capacitance
    - Type
  - Supply rail
    - Voltage
    - Ripple voltage as %
    - See appendix
  - Compute maximum supply current
    - Use early power estimator value
    - Or use Quartus II PowerPlay power analyzer maximum transient current to adjust transient current %

Calculating Target Impedance

- Altera target impedance (Zt) is calculated for each rail by dividing the allowed voltage deviation by the dynamic current drawn by the device
- The dynamic current is calculated to be 50% of the maximum current drawn, estimated from EPE

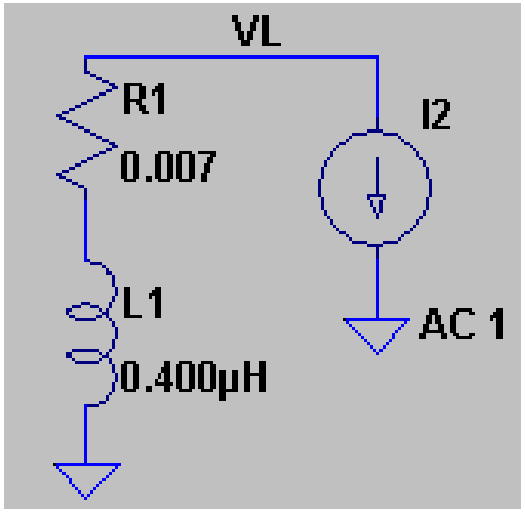
$$Z_{Target} = \left(\frac{V_{rail} \times \%\_ripple}{\frac{1}{2} I_{MAX}} \right) = \left(\frac{V_{ripple}}{\frac{1}{2} I_{MAX}} \right)$$

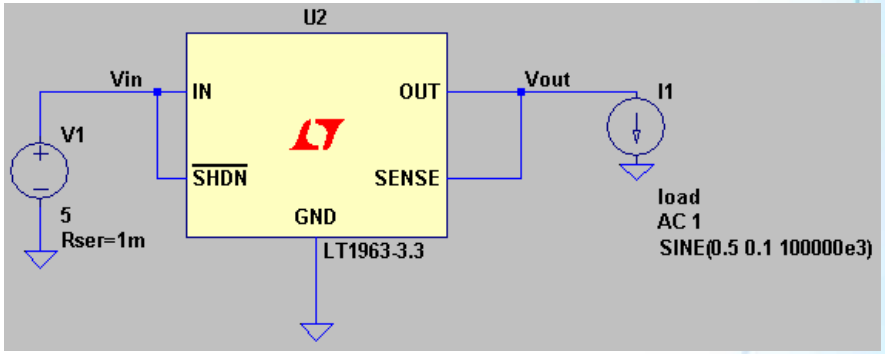
- PowerPlay power analyzer in Quartus II software provides the maximum dynamic current

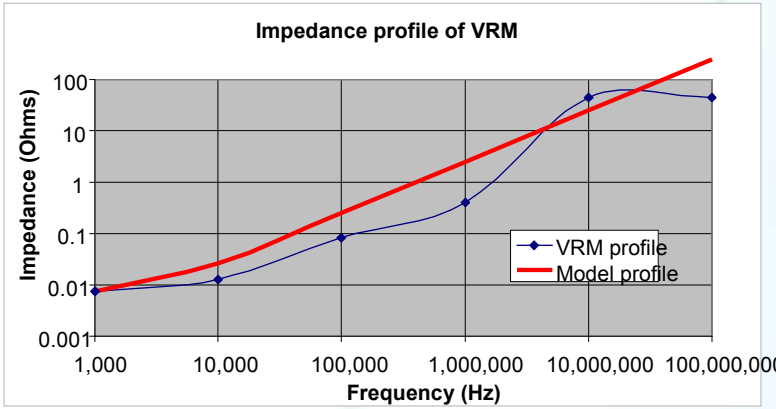
$$Z_{Target} = \left(\frac{V_{rail} \times \%\_ripple}{I_{MAX\ dynamic}} \right) = \left(\frac{V_{ripple}}{I_{MAX\ dynamic}} \right)$$

Selecting Voltage Regulator Module

- The VRM has an impedance profile that behaves like an inductor and resistor in series
- Custom option in PDN tool to model any VRM







Package Choice – Stratix IV GX Device Package Plan

Device	F780 (29 mm)	F1152 (35 mm)	F1152 (35 mm)	F1517 (40 mm)	F1760 (43 mm)	F1932 (45 mm)
EP4SGX70	368, 28, 8		480, 56, 24			
EP4SGX110	368, 28, 8	368, 28, 16	480, 56, 24			
EP4SGX180	368, 28, 8	560, 44, 16	560, 44, 24	736, 88, 36		
EP4SGX230 1st device	368, 28, 8	560, 44, 16	560, 44, 24	736, 88, 36		
EP4SGX290	288, 0, 16	560, 44, 16	560, 44, 24	736, 88, 36	864, 88, 36	904, 98, 48
EP4SGX360	288, 0, 16	560, 44, 16	560, 44, 24	736, 88, 36	864, 88, 36	904, 98, 48
EP4SGX530 2nd device			560, 44, 24	736, 88, 36	864, 88, 36	904, 98, 48

Pin migration

Total I/O, LVDS, transceiver counts

14-layer package substrate with increased on-package decoupling (OPD)

Notes:
Flip-chip ball-grid array (BGA) with 1.0-mm pitch
Details subject to change

EP4SGX230HF35C4(N)

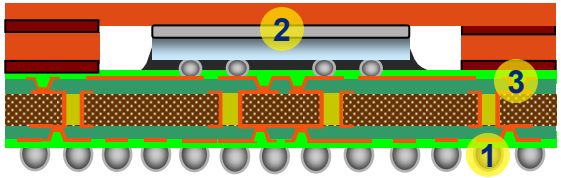
H, K, N all have enhanced OPD

Package and Die Features

Supply	$f_{effective}$	
	EP4SGX230FF35 (8 layers)	EP4SGX230HF35 (14 layers)
VCC	~25 MHz	~24 MHz
VCCA_(L/R)	80 MHz	~20 MHz
VCCR_(L/R)	~50 MHz	~20 MHz
VCCT_(L/R)	~50 MHz	~20 MHz
VCCHIP_(L/R)	80 MHz	~60 MHz

Typical maximum frequency needed to be decoupled for different Stratix IV GX packages (This is device dependent. You need to use the PDN tool.)

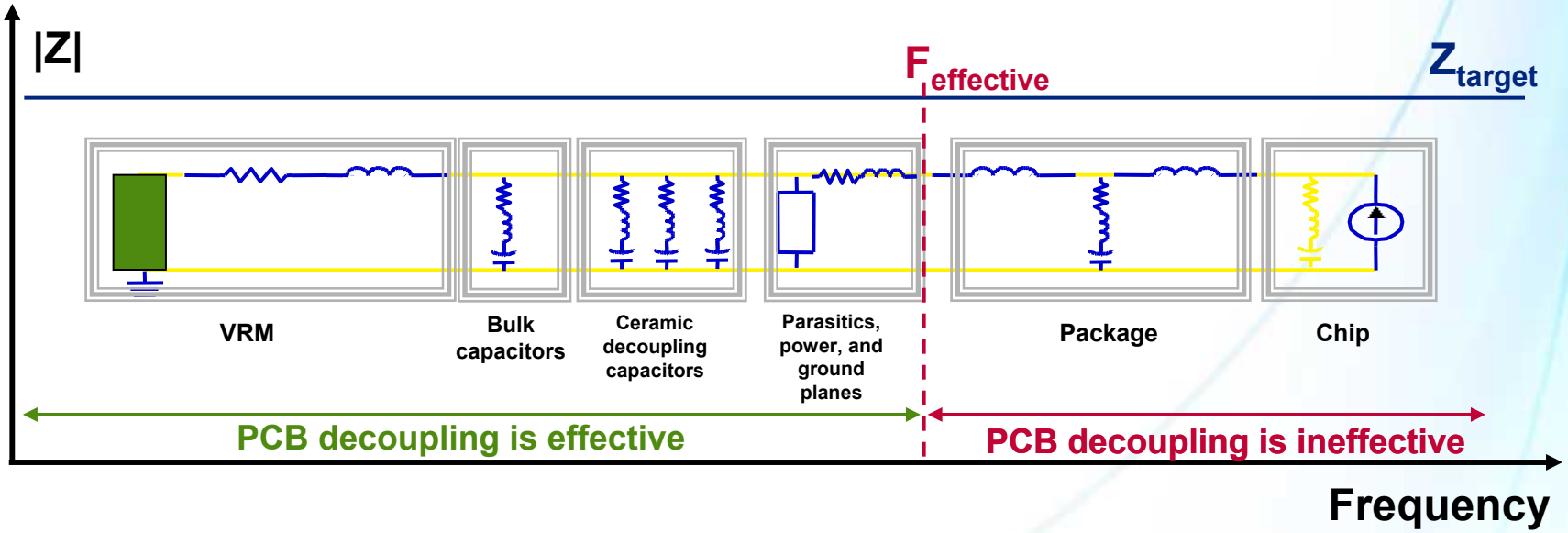
Note: preliminary data



Silicon and package features	Benefits
1. 8:1:1 – I/O:GND:PWR ratio 2. On-die decoupling capacitors 3. On-package decoupling capacitors	1. Reduces loop inductance → reduces SSN 2. Improves power quality 3. Improves power quality

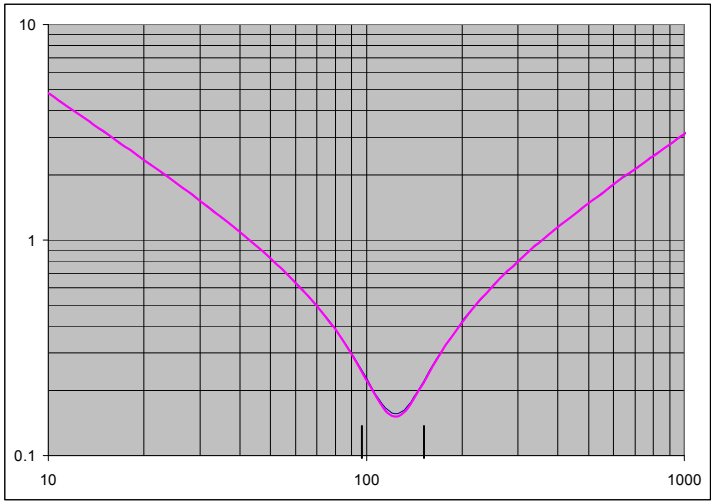
Use $f_{effective}$ to Reduce Over-Design

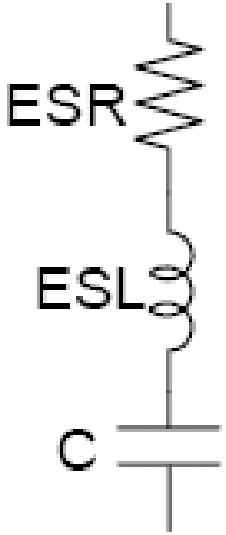
- PCB decoupling capacitors are ineffective in reducing PDN |Z| beyond $f_{effective}$
  - PCB capacitors are limited due to system ESL
  - Device OPD/ODC dominate at high frequencies
- $f_{effective}$ is device specific
  - $f_{effective}$ calculation takes die, package, and PCB parasitics



Properties of Decoupling Capacitor

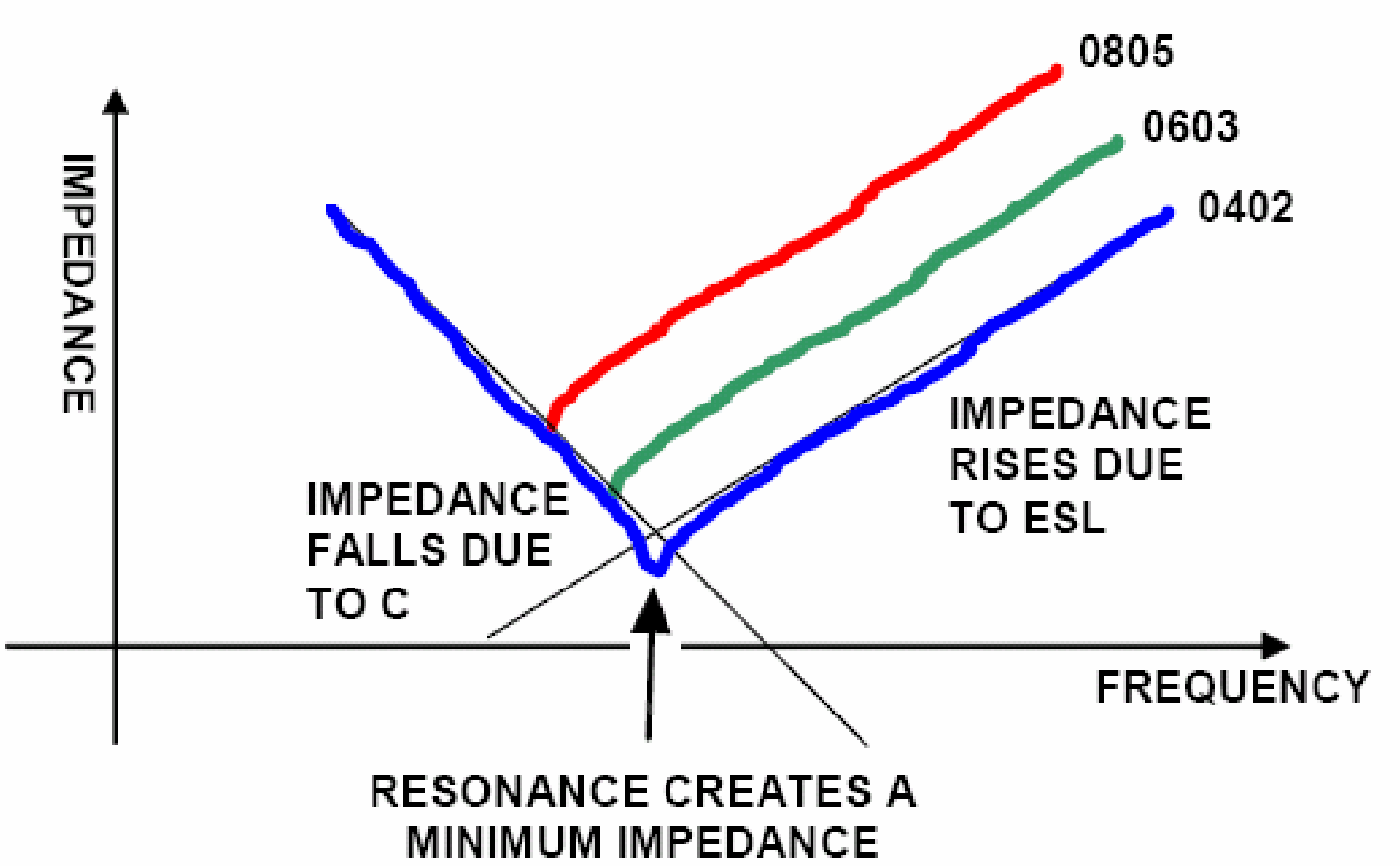
- The most effective area of decoupling occurs within the bandwidth of any given capacitor



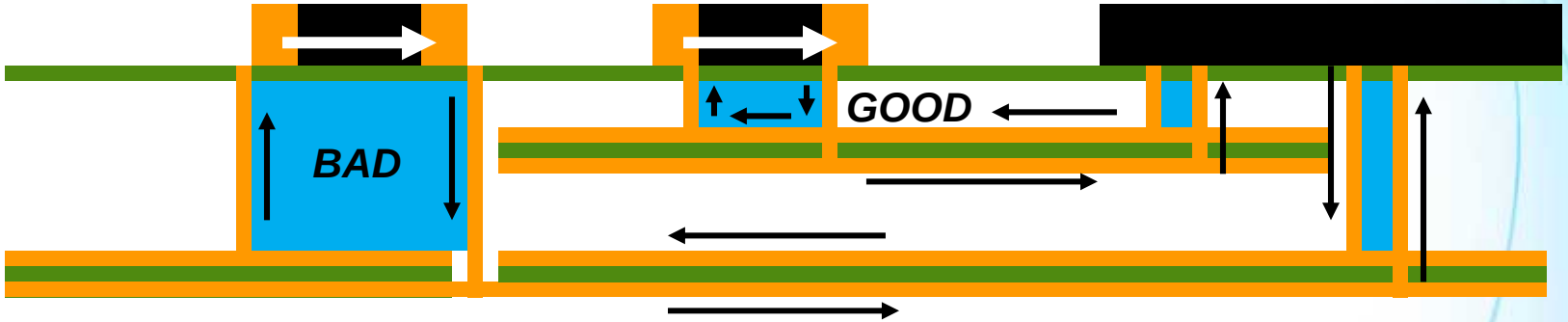


$$SRF = \frac{1}{2\pi\sqrt{C * ESL}}; \quad Q = \frac{\sqrt{\frac{ESL}{C}}}{ESR} \quad ; \quad BW = SRF/Q$$

Z Profile vs. Package

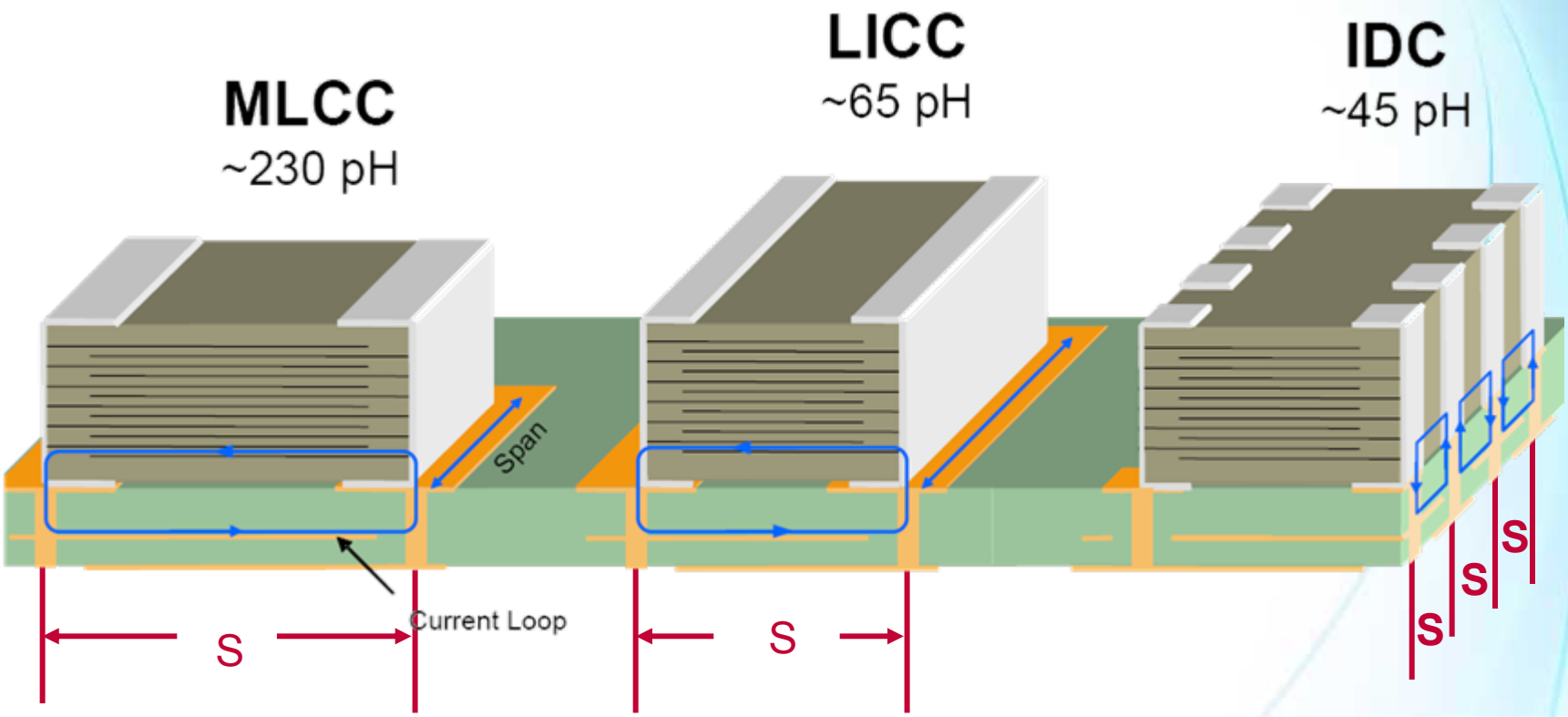


Mounting Inductance



- Reduce mounting inductance
  - Place capacitor as close as possible to load
  - Place capacitor on load side of board
  - Place power plane for power delivery close to load
  - Place power and GND planes adjacent for interplane capacitance
  - Place vias to power and ground on capacitor as close as possible

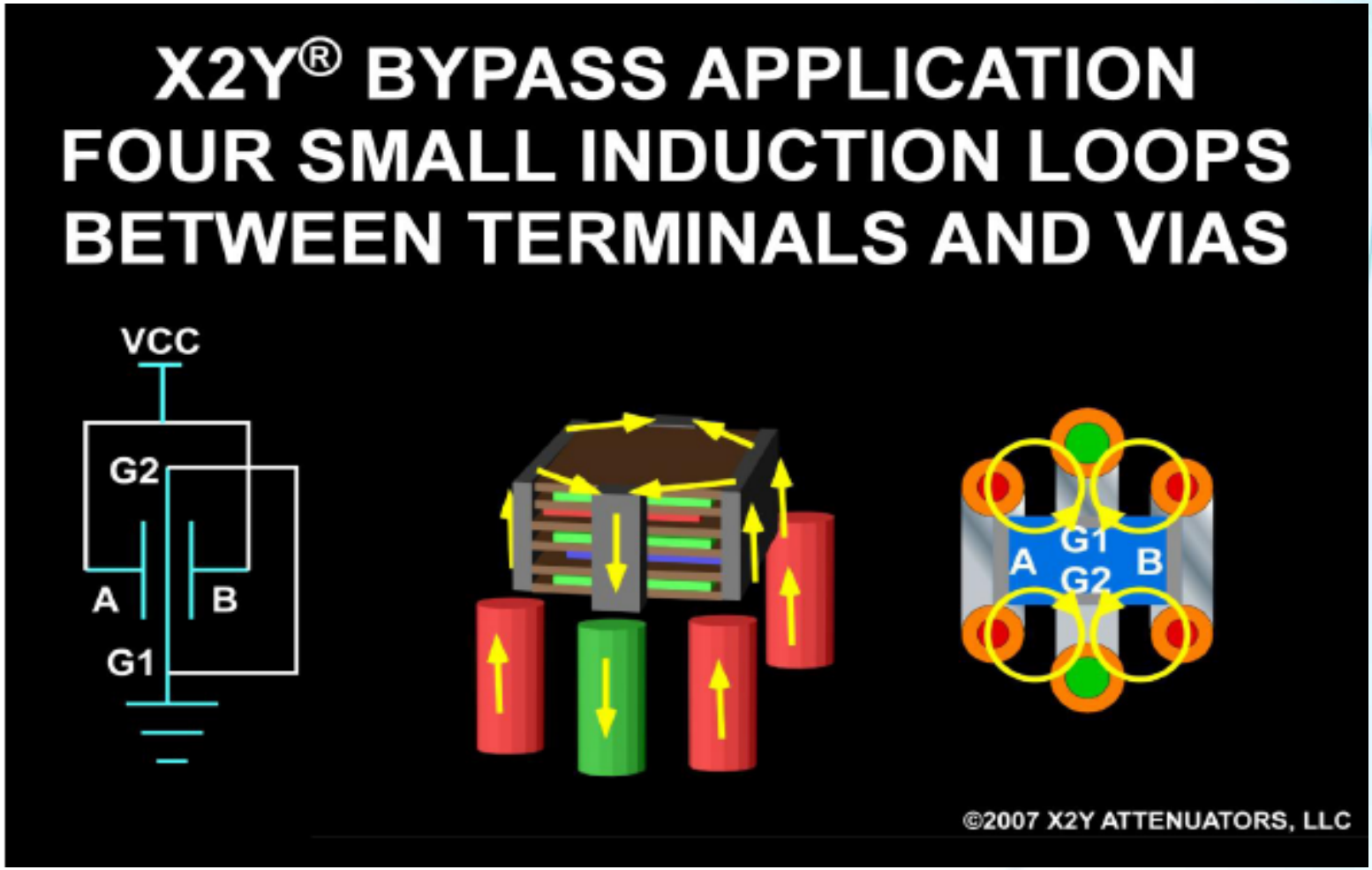
Loop Inductances and Capacitor Geometry



$$L_{vias} = 10.16 \times h_{top} \times \ln\left(\frac{2S}{D}\right) pH$$

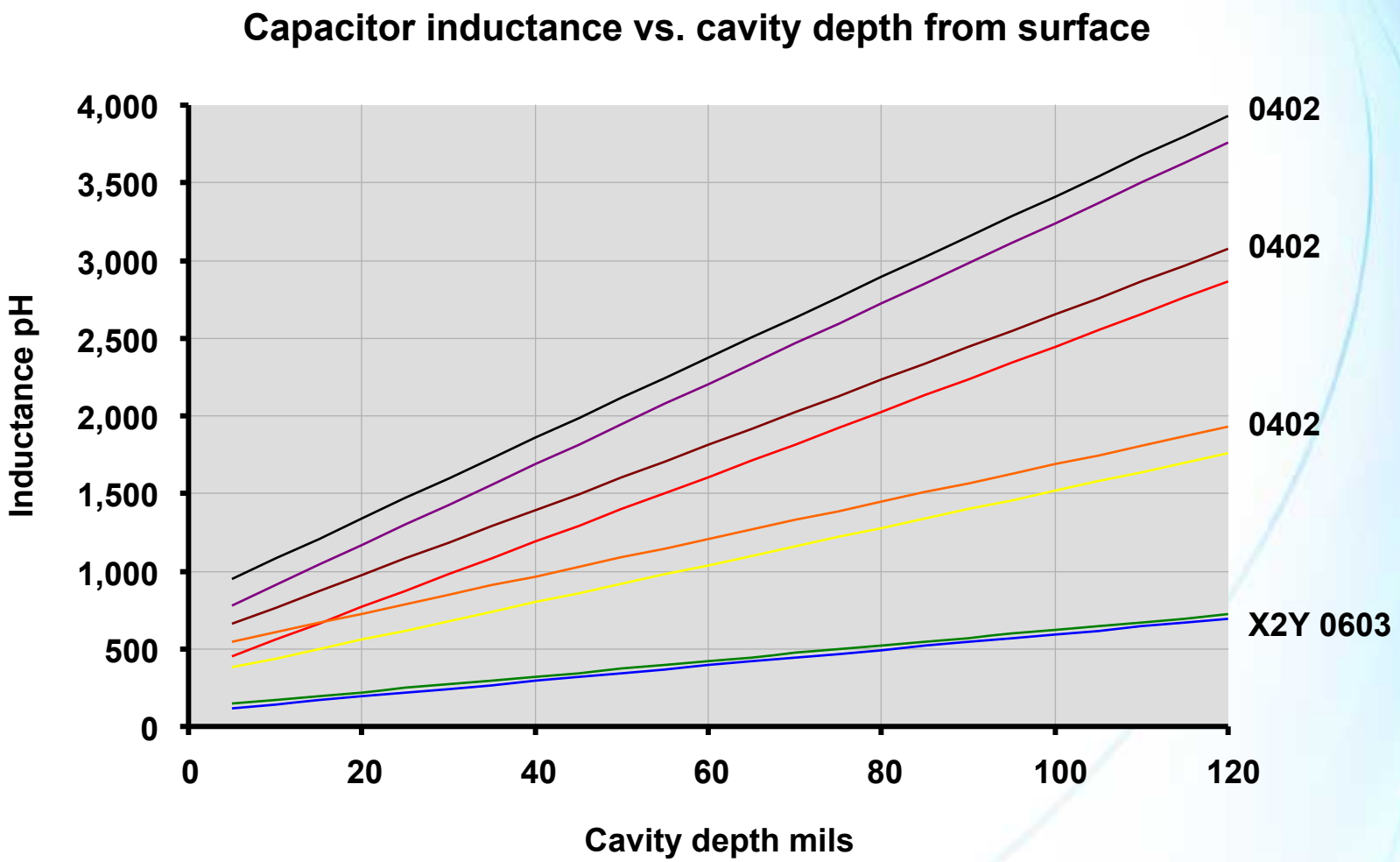
Courtesy of AVX

Loop Inductance on X2Y Geometry



Courtesy of X2Y

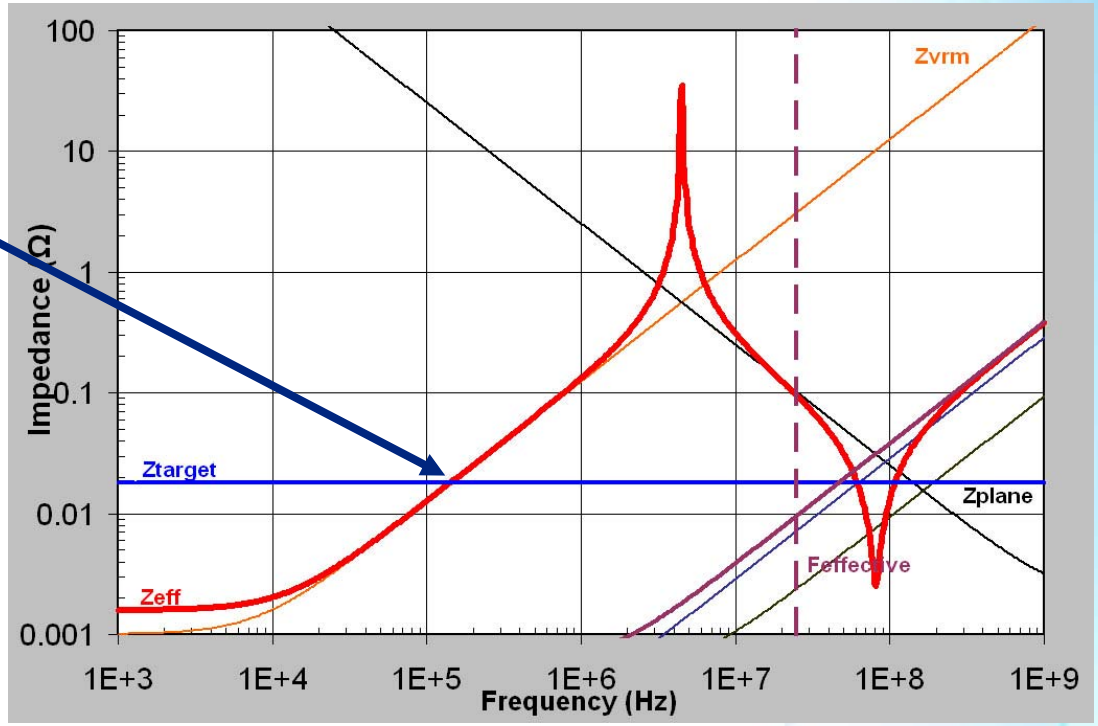
Capacitor Geometry and Inductive Loops



Courtesy of X2Y

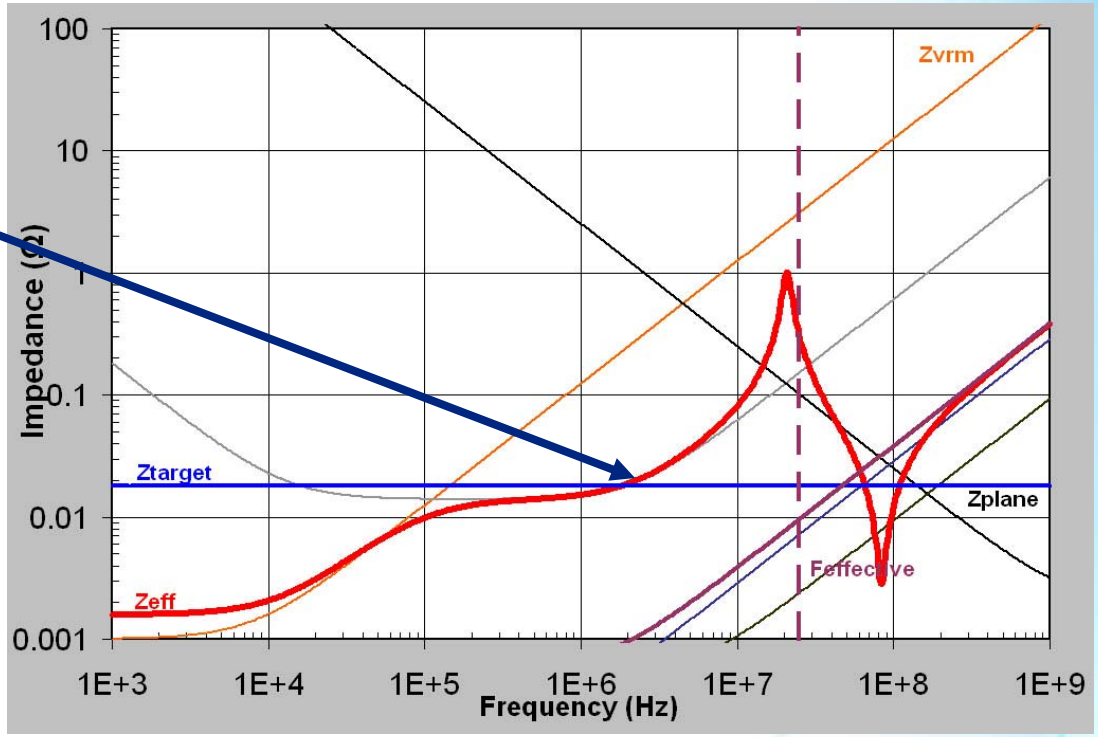
Bypass Capacitor Selection Methodology, Part 1

- Select VRM
- Start at the lowest frequency where Z_{eff} crosses Z_{target}
- ~150 kHz
- Add large capacitors until $Z_{eff} < Z_{target}$ at target frequency



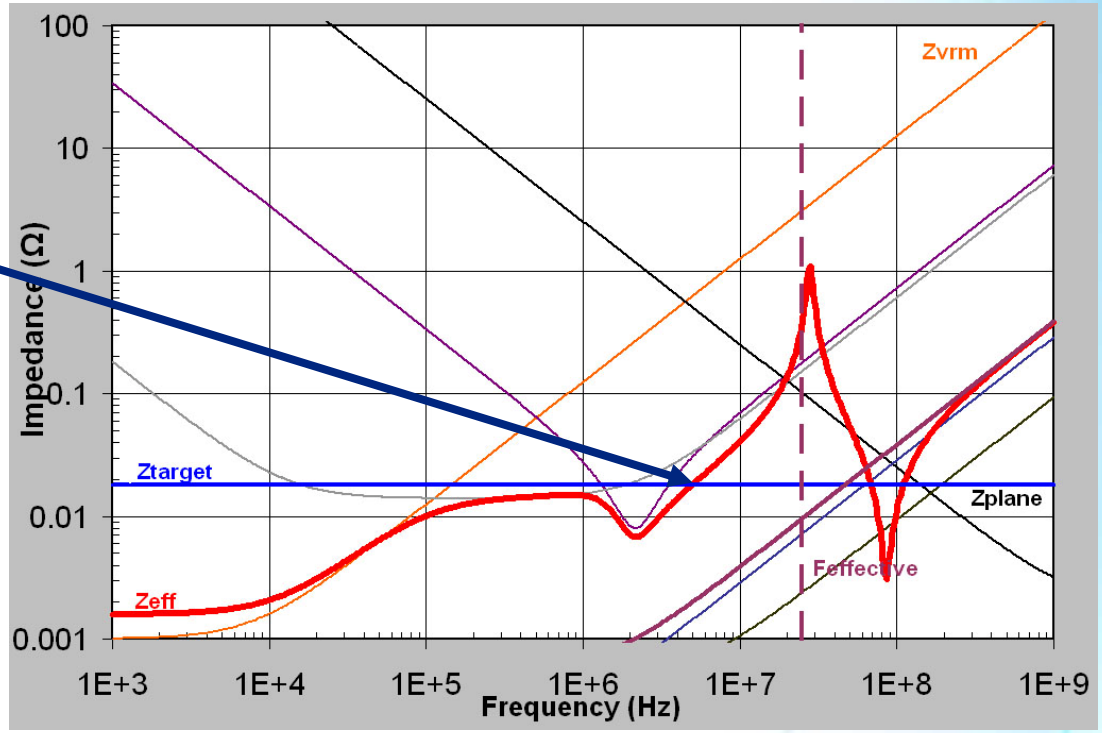
Bypass Capacitor Selection Methodology, Part 2

- Added 4 x 220µF bulk capacitors
- New crossing point
- Add smaller capacitors



Bypass Capacitor Selection Methodology, Part 3

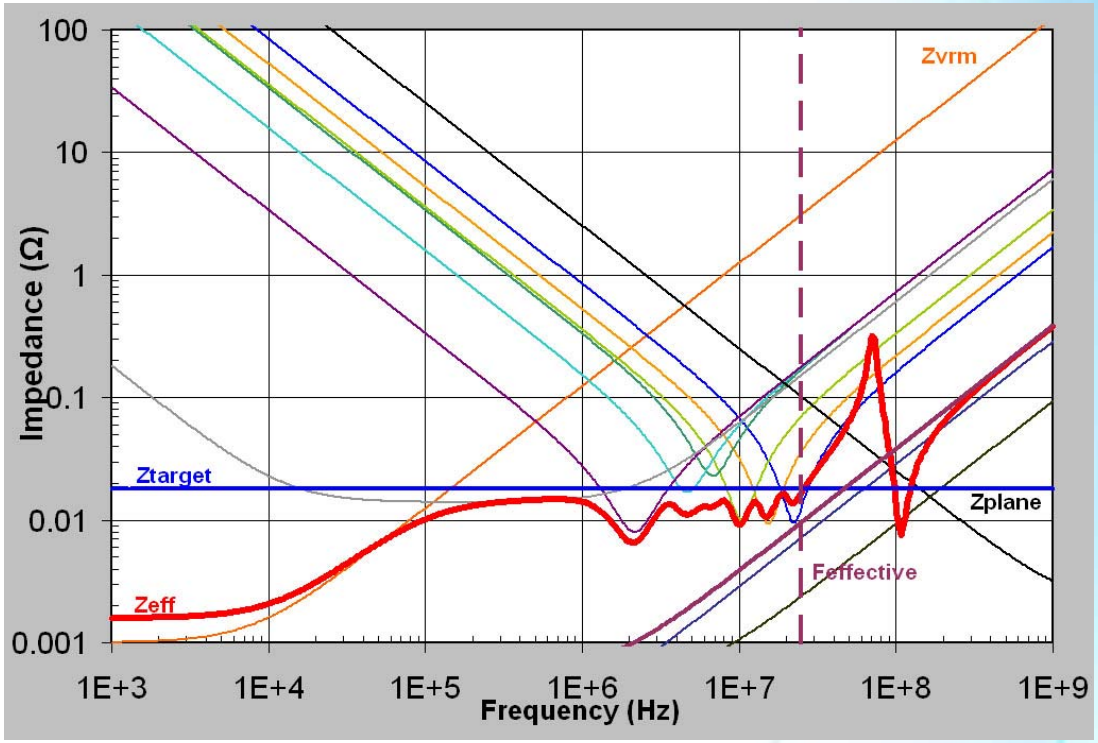
- 4 x 220µF bulk capacitors, 1 x 4.7µF MLCC capacitor
- New crossing point
- Add smaller capacitors
- Until crossing point ≥ past $f_{effective}$



Bypass Capacitor Selection Methodology, Part 4

- Final bypass capacitor selection

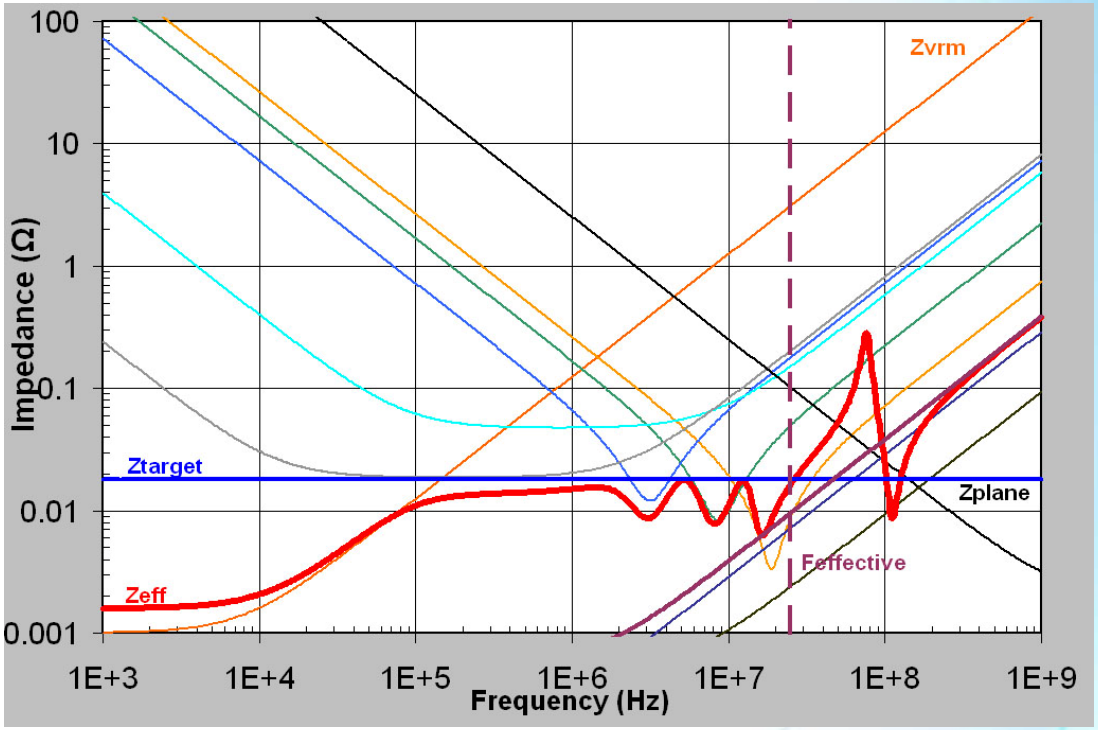
4 x 220µF bulk cap
1 x 4.7µF MLCC 0603
1 x 1µF MLCC 0603
1 x 0.47µF MLCC 0603
2 x 0.22µF MLCC 0402
3 x 100nF MLCC 0402
4 x 47nF MLCC 0402
Total 15 caps



Bypass Capacitor Selection Methodology, Part 5

- Final bypass capacitor selection, alternative solution

3 x 220µF bulk cap
4 x 10µF bulk cap
1 x 2.2µF MLCC 0603
1 x 0.47µF MLCC 0603 X2Y
3 x 100nF MLCC 0603 X2Y
Total 12 caps



Many different solutions – still needs engineering skill for optimal solution

Summary

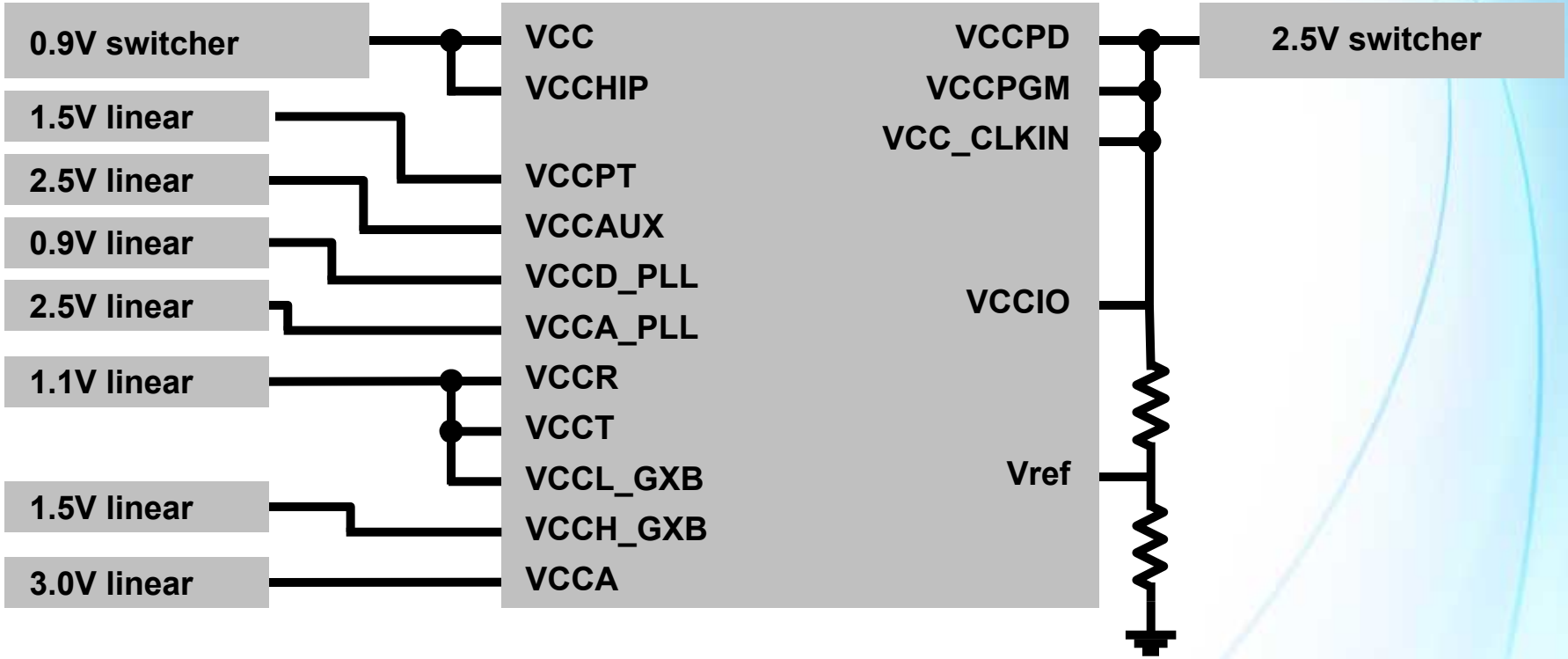
- Innovative architecture and advanced process technologies ease PDN design
  - Programmable Power Technology
  - Stratix IV GX FPGAs - lowest power, high-performance FPGAs
  - Arria II GX FPGAs - lowest power, cost-optimized FPGAs with up to 3.75-Gbps transceivers
- Best-in-class FPGA power modeling
  - Early power estimator and Quartus II PowerPlay power analyzer
    - Accurate power estimator
    - Allows power optimization
- Ease of design with Altera's PDN tool
  - Fairly accurate, easy-to-use spreadsheet tool
  - Provides a scientific way (FDTIM) to decouple power rails in the system
  - As accurate as the inputs provided by the user
  - Has proved very useful while designing PDN for Altera boards

More Information

- Board Design Resource Center
  - PDN tool
  - Channel design guidelines
  - PCB and stack-up design considerations
  - Memory interfacing, thermal considerations, and much more
  - www.altera.com/board
- Power distribution network design tool
  - Altera PDN Design Tool
  - Altera PDN Design Tool User Guide
  - Online training - Power Distribution Network Design for Stratix III and Stratix IV FPGAs
  - For more information on FDTIM (method behind PDN tool), refer to *Comparison of Power Distribution Network Design Methods* (PDF)

Appendix

Stratix IV GX Power Rails



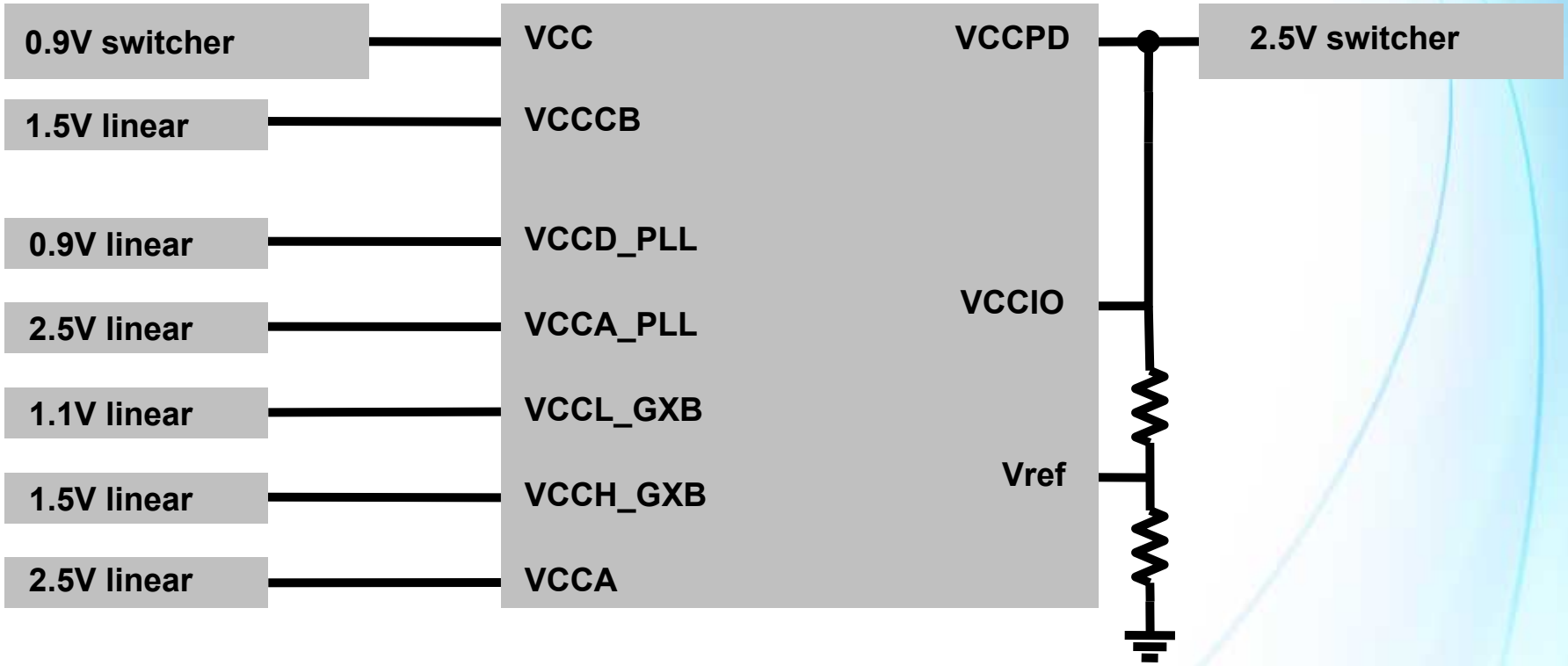
VCCBAT not shown

Stratix IV GX Power Rails (Min. Combined)

No	Rail name	Voltage	Voltage ripple tolerance	Description
1	VCC	0.9V	⌖3.3%	Core and periphery
	VCCHIP	0.9V	⌖5%*	*Transceiver PCI Express hard IP block
2	VCCPD	2.5V	⌖5%	I/O pre-drivers
	VCCPGM	2.5V	⌖5%	Configuration I/Os
	VCC_CLKIN	2.5V	⌖5%	VIO clock input pins
3	VCCPT	1.5V	⌖3.3%	Programmable Power Technology
4	VCCAUX	2.5V	⌖5%	Programmable Power Technology aux.
5	VCCD_PLL	0.9V	⌖3.3%	PLL digital
6	VCCA_PLL	2.5V	⌖5%	PLL analog
7	VCCR	1.1V	⌖5%	Transceiver analog receive
	VCCT	1.1V	⌖5%	Transceiver analog transmit
	VCCL_GXB	1.1V	⌖5%	Transceiver clock distribution
8	VCCH_GXB	1.5V	⌖5%	Transceiver block buffers
9	VCCA	3.0V	⌖5%	Transceiver analog Tx/Rx driver
10	VCCIO[23:0]	1.2V-3.0V	⌖5%	24 I/O banks

*** If connected to VCC – supply must support tighter VCC tolerance (3.3%)**

Arria II GX Power Rails



VCCBAT not shown

Arria II GX Power Rails (Min. Combined)

No	Rail name	Voltage	Voltage ripple tolerance	Description
1	VCC	0.9V	⌖3.3%	Core, periphery, PCIe hard IP, and transceiver PCS
2	VCCPD	2.5V	⌖5%	I/O pre-drivers
3	VCCCB	1.5V	⌖5%	Configuration RAM supply
4	VCCD_PLL	0.9V	⌖3.3%	PLL digital supply
5	VCCA_PLL	2.5V	⌖5%	PLL analog supply
6	VCCL_GXB	1.1V	⌖5%	Transceiver PMA Tx/Rx and clock supply
7	VCCH_GXB	1.5V	⌖5%	Transceiver PMA Tx buffer supply
8	VCCA	2.5V	⌖5%	Transceiver PMA regulator supply
9	VCCIO[23:0]	1.2V-3.0V	⌖5%	24 I/O banks