



# Altera Technical Solutions Seminar 2000



# Schedule

- Opening
- Introduction
- FLEX<sup>®</sup> 10KE Devices
- APEX<sup>™</sup> 20K & Quartus<sup>™</sup> Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo



# Agenda

- u About Altera
- u Need for Speed
- u New Architectures
- u New Design Tools



## Introduction

FLEX<sup>®</sup> 10KE Devices

APEX<sup>™</sup> 20K &  
Quartus<sup>™</sup> Overview

Design Integration

EDA Integration

Intellectual Property

Design Iteration

Design Optimization

Internet Interface

Roadmap

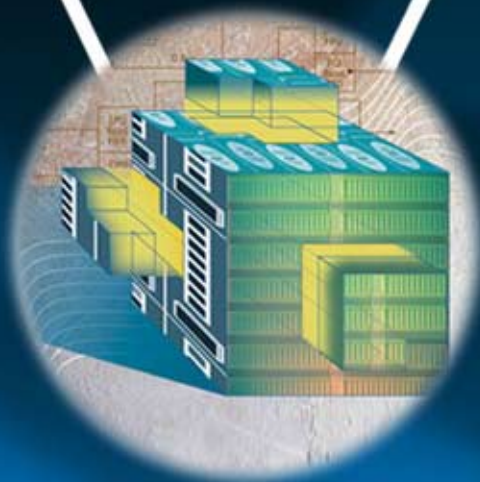


# Altera's Mission

**High-Density  
CMOS  
Programmable  
Logic Devices**



**Design  
Tools**



**Intellectual Property**



# Highlights

- ◆ Founded in 1983
- ◆ \$837 Million in 1999 Sales
- ◆ 1,100+ Employees
- ◆ 13,000+ Customers Worldwide



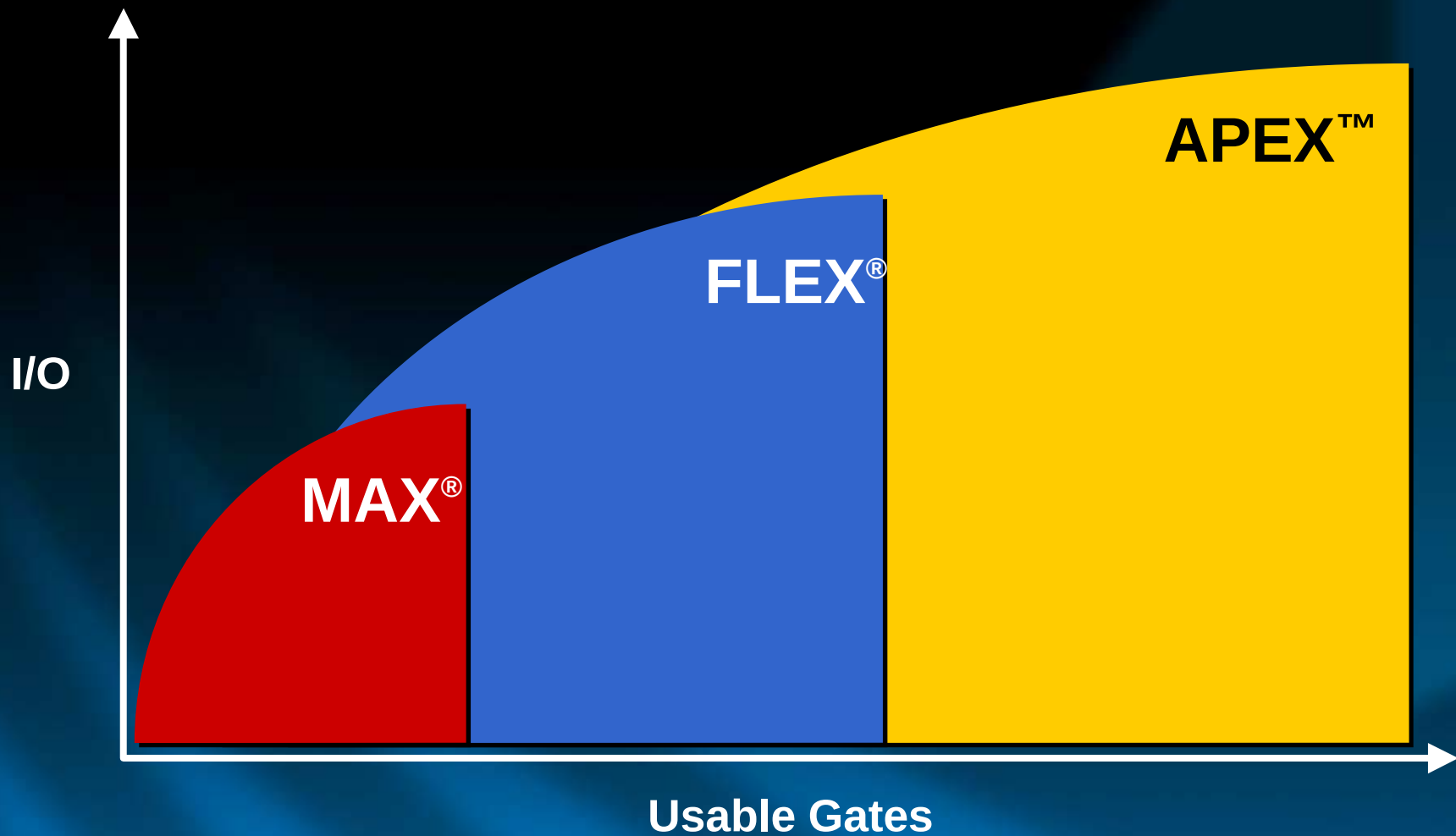


# Altera Sales Offices



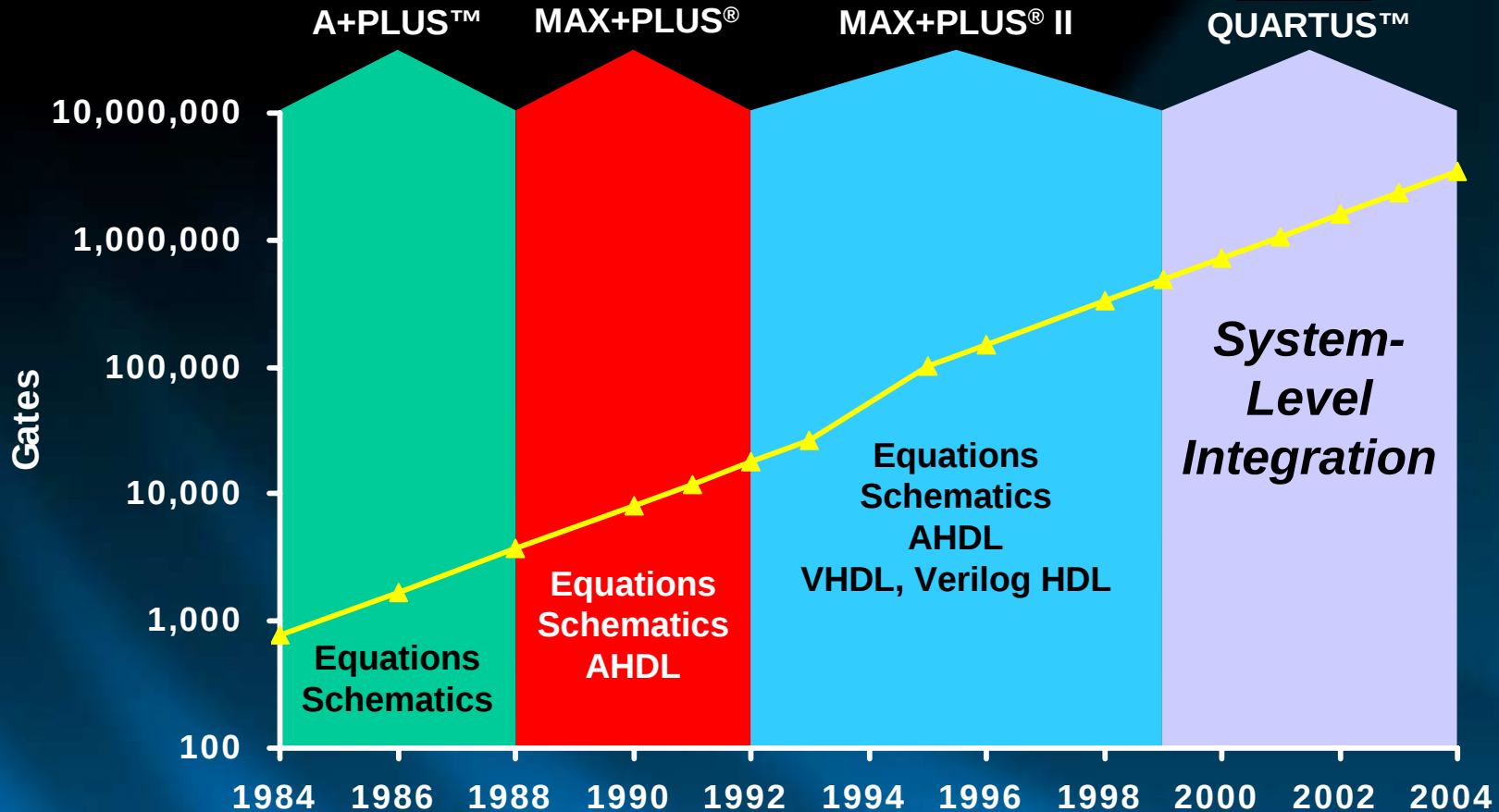


# Product Overview





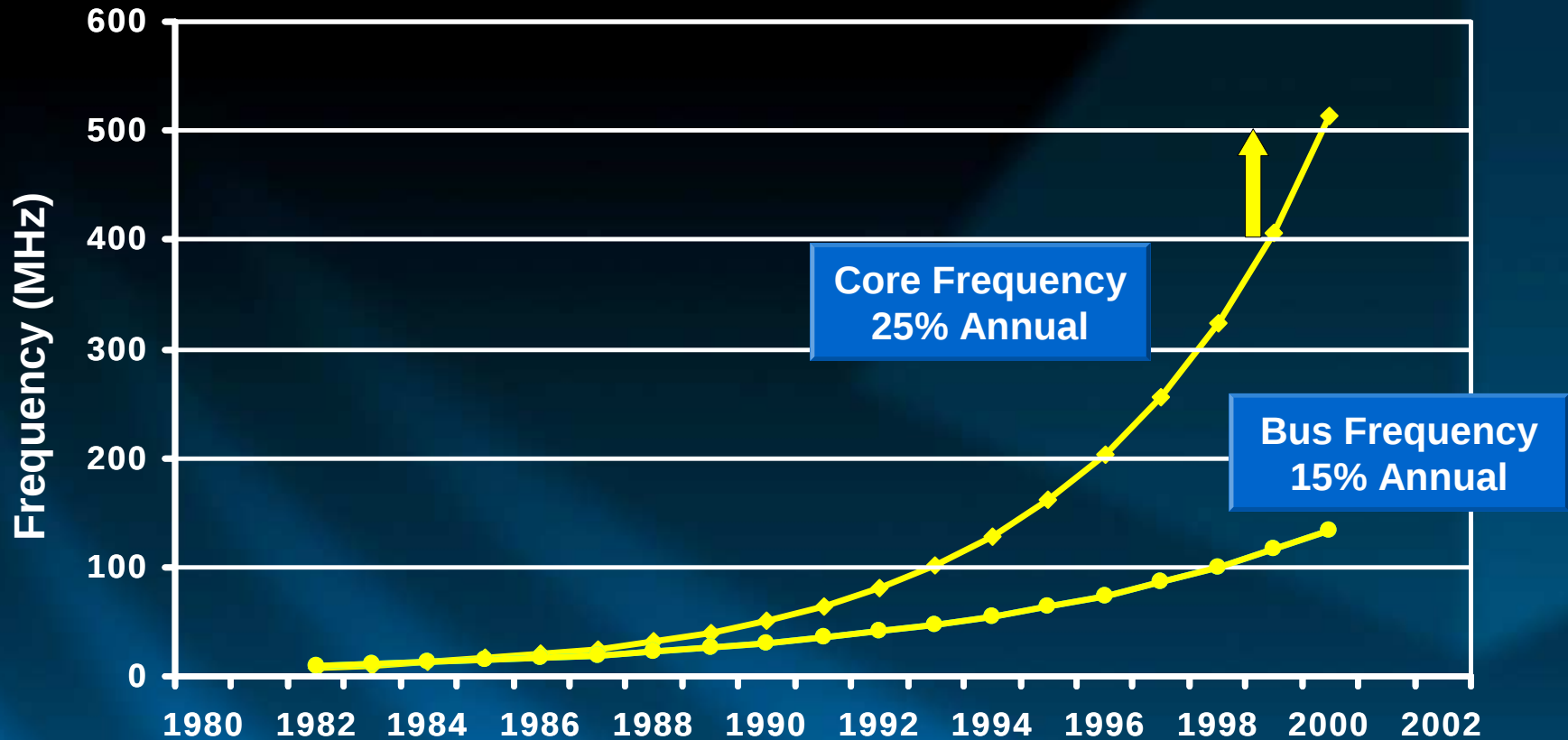
# Design Tool Evolution





# Technology Is Driving Performance

X86 Microprocessor & System Bus Frequency





# The Need for Speed



Source: Dataquest



ALTERA®



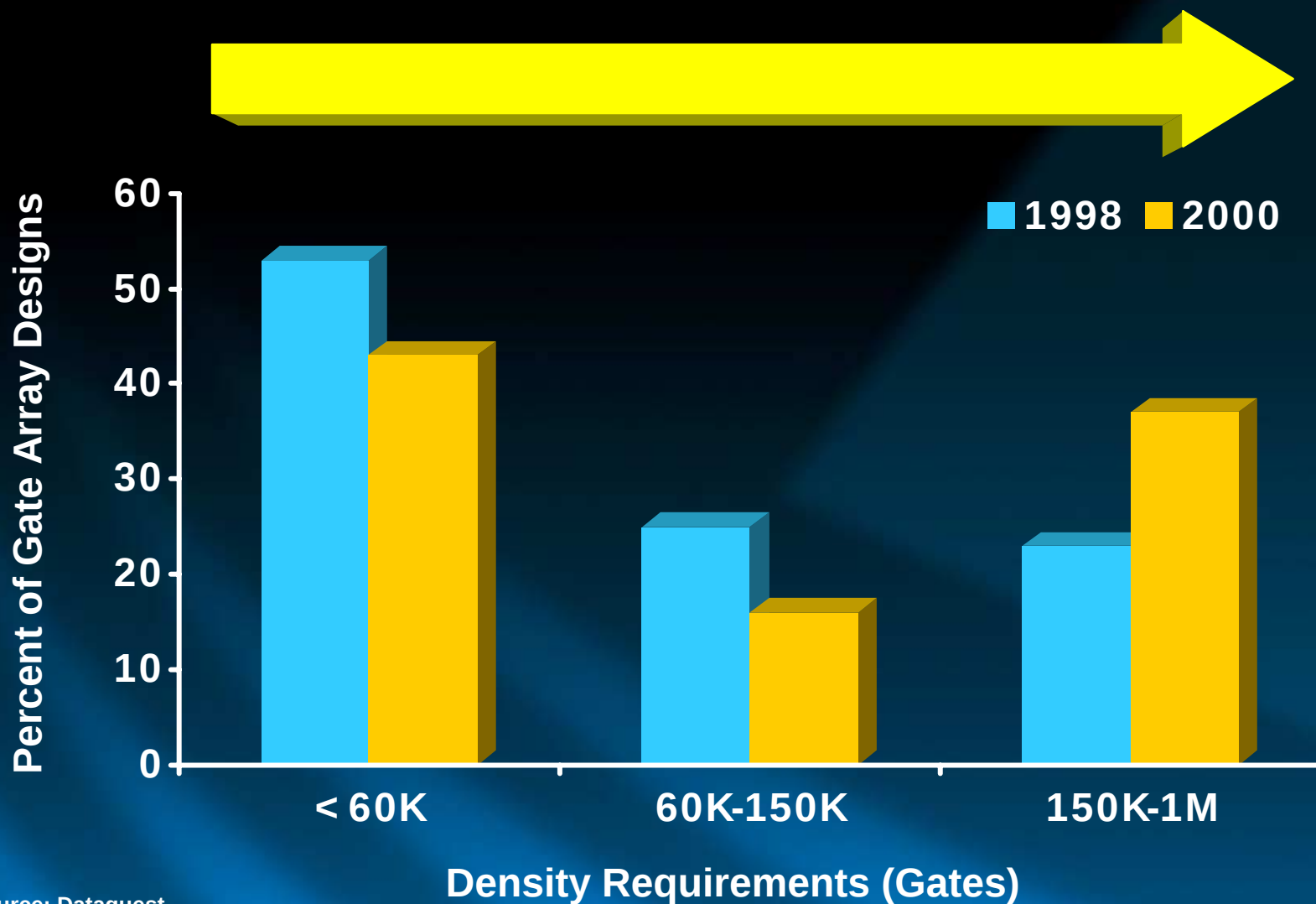
# FLEX 10KE Devices Push Performance

- ◆ 115-MHz System Speeds
- ◆ 64-Bit, 66-MHz PCI Compliance
- ◆ Up to 200,000 Gates





# The Need for Density



Source: Dataquest





# APEX Architecture Capabilities

## DESIGN SIZE

- 2-Million-Gate Designs

## SYSTEM PERFORMANCE

- 125-MHz Requirements



## SYSTEM ENVIRONMENTS

- Low Voltage
- Bus Protocols
- I/O Standards

## SYSTEM-LEVEL FUNCTIONS

- Memory
- PLL
- ASSP Integration



# Quartus Software Capabilities

## LARGER, FASTER DEVICES

- 2-Million-Gate Designs
- Higher Performance

## TIME TO MARKET

- HDL-Based with IP
- Third-Party Tools Predominant
- Workgroup Computing



## COMPUTING ENVIRONMENT

- Windows NT and UNIX
- Multi-Processor Systems
- Heterogeneous Networks
- Distributed Computing

## SOFTWARE TECHNOLOGIES

- Object-Oriented Databases
- World-Wide Web
- COM



# Satisfying ASIC and PLD Users

## TRADITIONAL PLD USER

- n Easy-to-Use Tools
- n Simple Design Methodology
- n Fast Compilation Times

## GATE ARRAY DESIGNER

- n Sophisticated, Powerful Tools
- n Use Existing EDA Tool Flow



## HIGH-DENSITY PLDs

- n Increasing Densities
- n Increasing Design Complexity
- n New Design Methods



# Meeting the Needs of the Future Today

- ◆ **FLEX<sup>®</sup> 10KE Devices**
- ◆ **APEX<sup>™</sup> 20K Devices**
- ◆ **Quartus<sup>™</sup> Development Tools**