Altera Technical Solutions Seminar 2000

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Schedule

- Opening
- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo

Agenda

- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- **Design Integration**
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap

- MultiCore™ Architecture
- I/Os
- ClockLock™, ClockBoost™ Circuitry
- Workgroup Computing
- Multi-Processor Fitting

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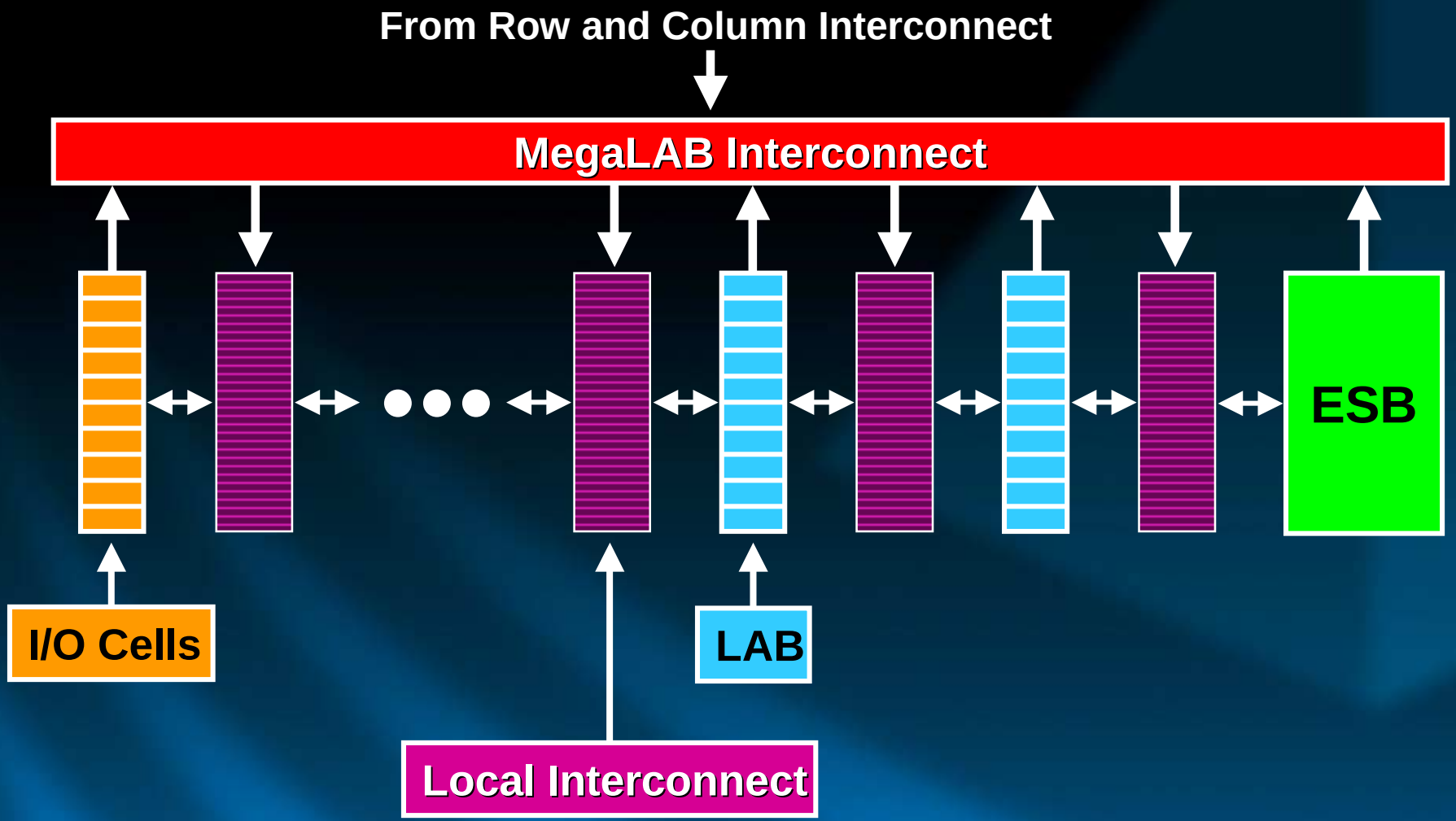
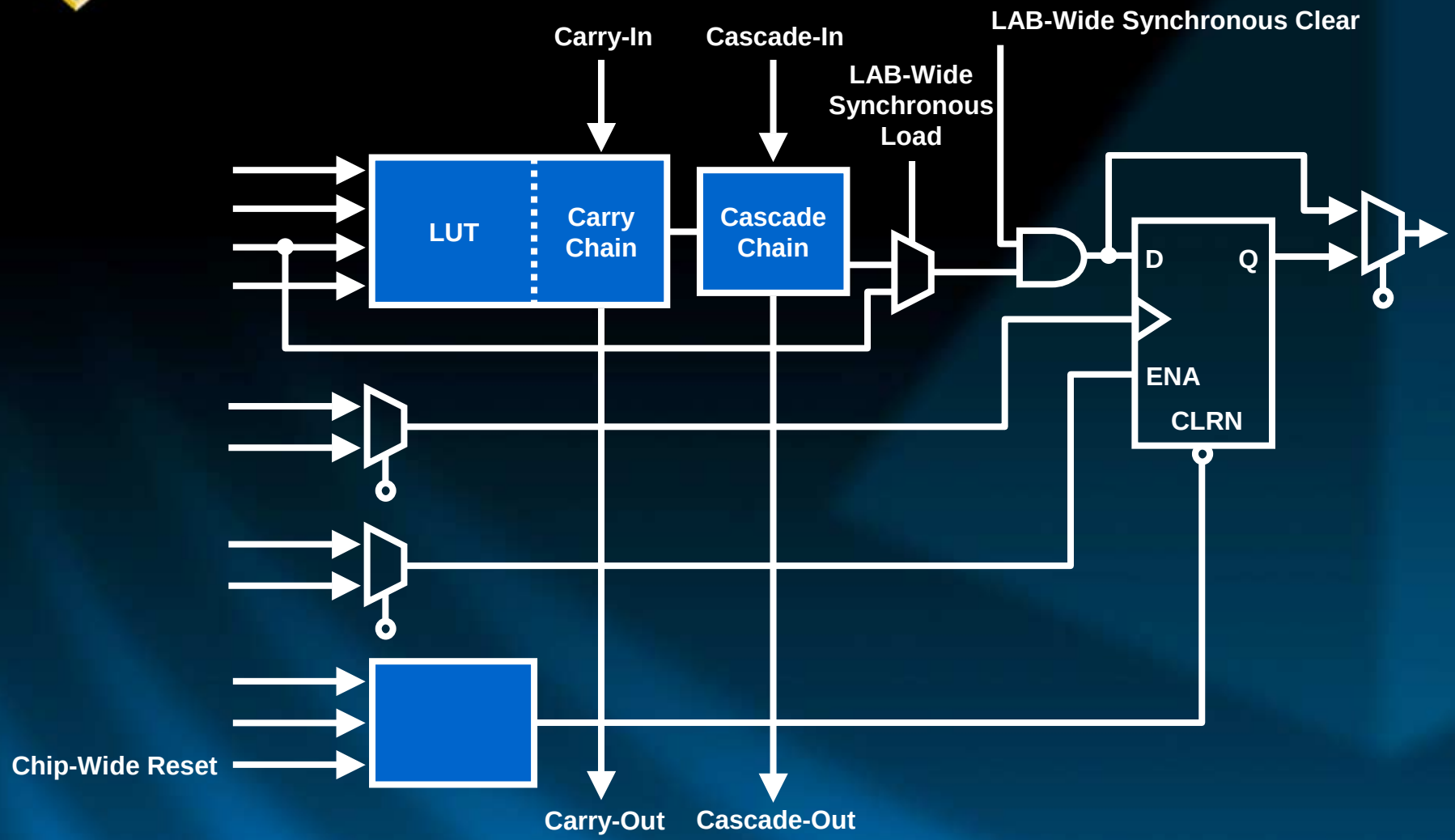
MultiCore Architecture

- LUTs for Logic
- Product Terms for Logic
- Memory for:
  - RAM
  - FIFO
  - CAM
  - ROM

MegaLAB: New Level of Hierarchy

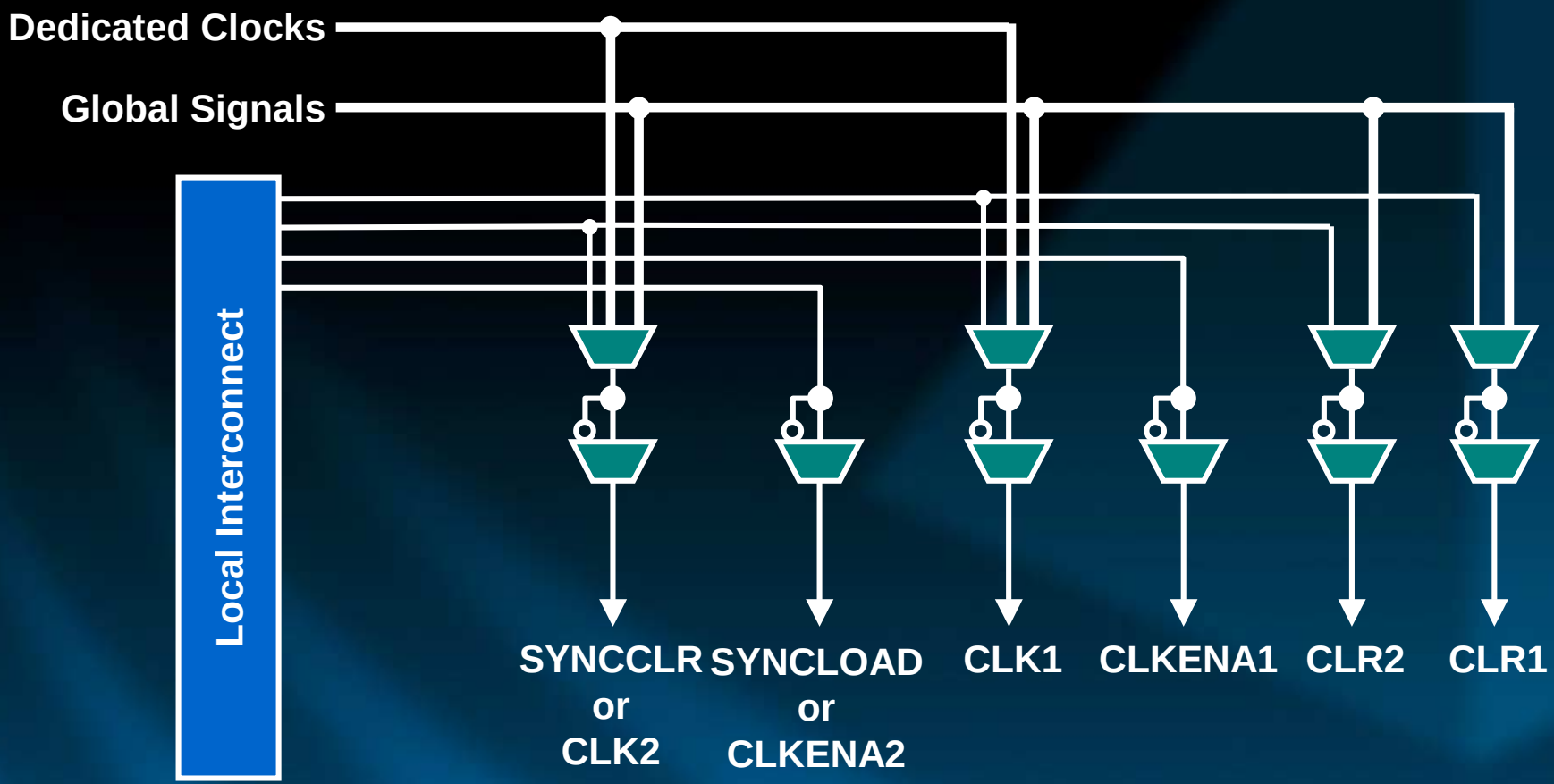


LE Structure



Superset of FLEX 6000, FLEX 10K Features

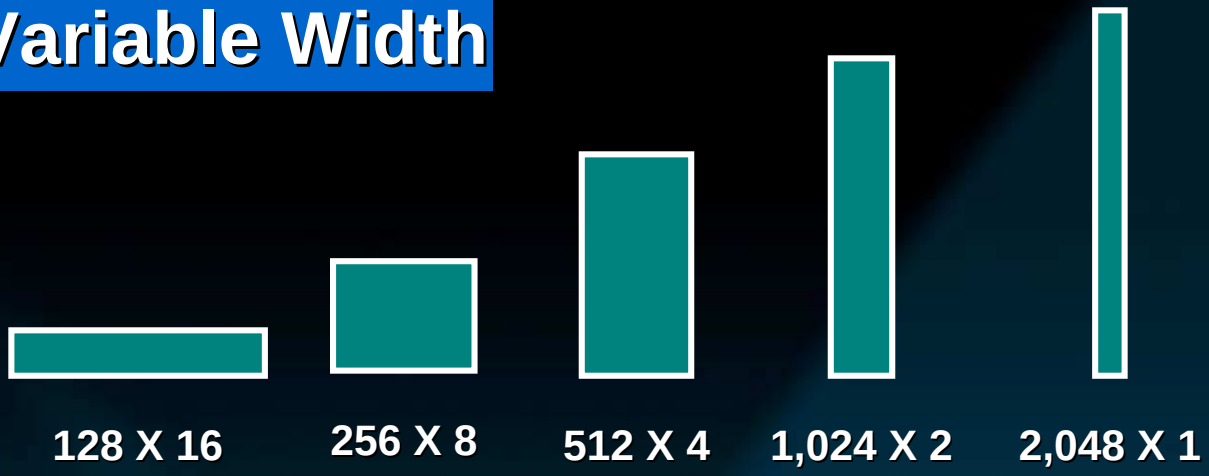
Control Signal Flexibility



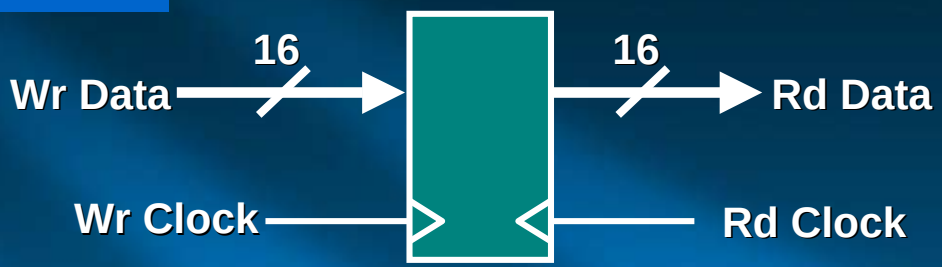
Embedded System Block

Embedded RAM

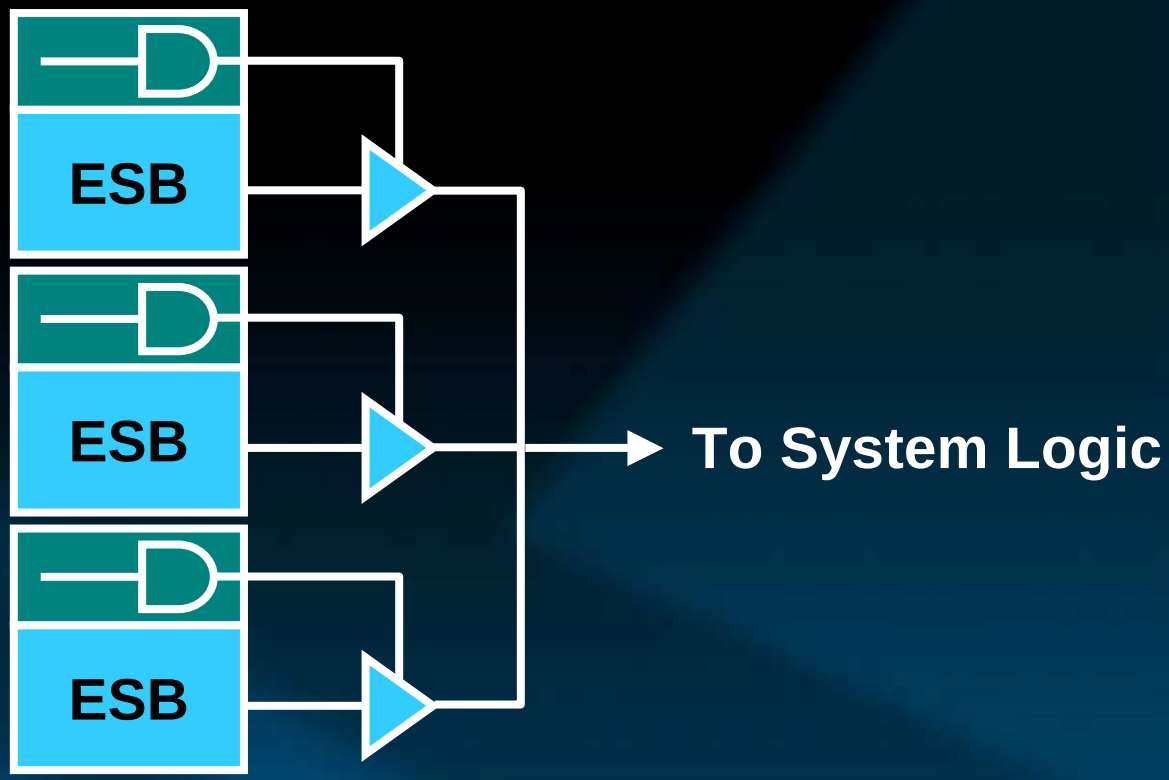
Variable Width



Dual-Port



Creating Deeper Memories



Required Address Decodes Built into ESB

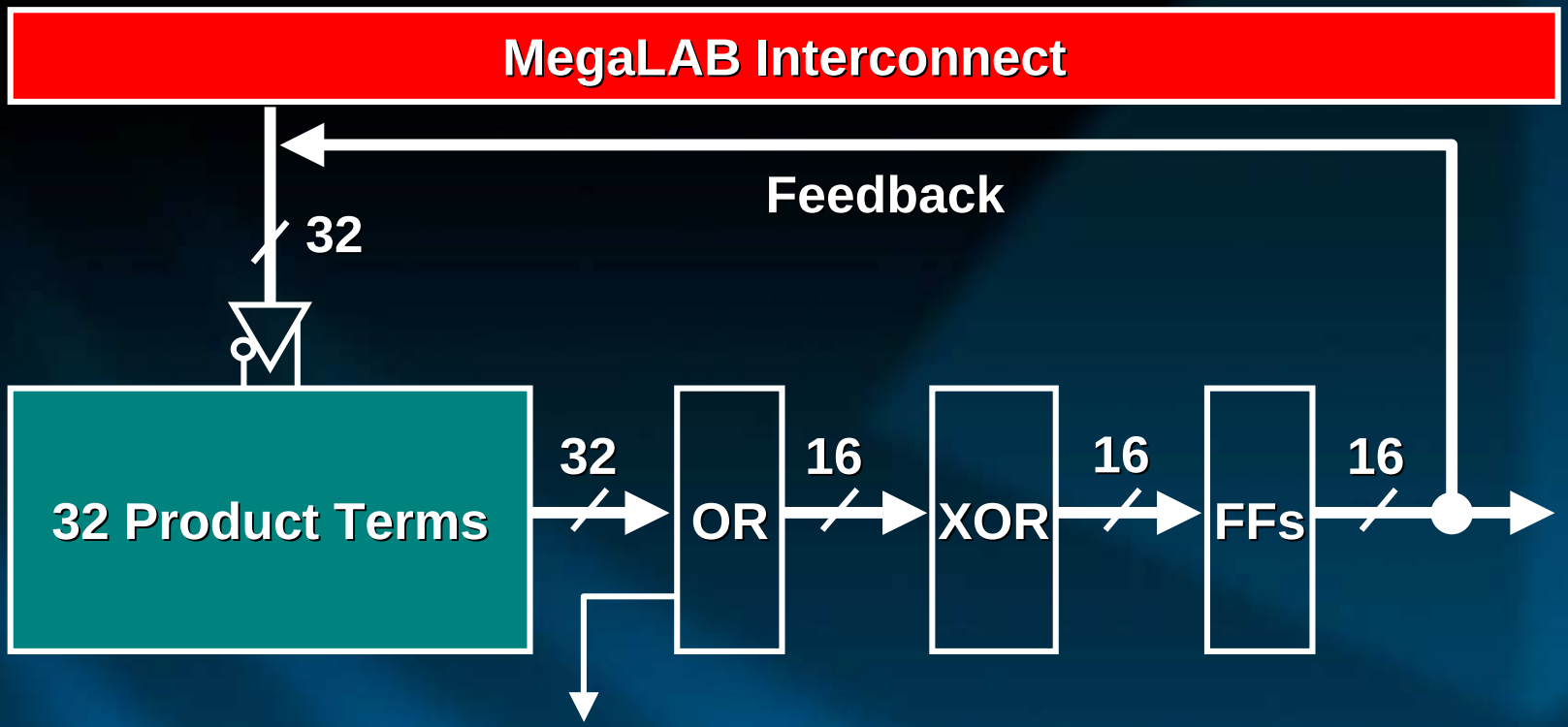
System-Level Memory Integration

Function	Configuration	Total ESBs	Performance
Cache RAM	256 x 32 4,096 x 64	4 128	161 MHz 151 MHz
Dual-Port FIFO	128 x 32 128 x 64	2 4	161 MHz 161 MHz
ROM	256 x 32 4,096 x 64	4 128	227 MHz 207 MHz

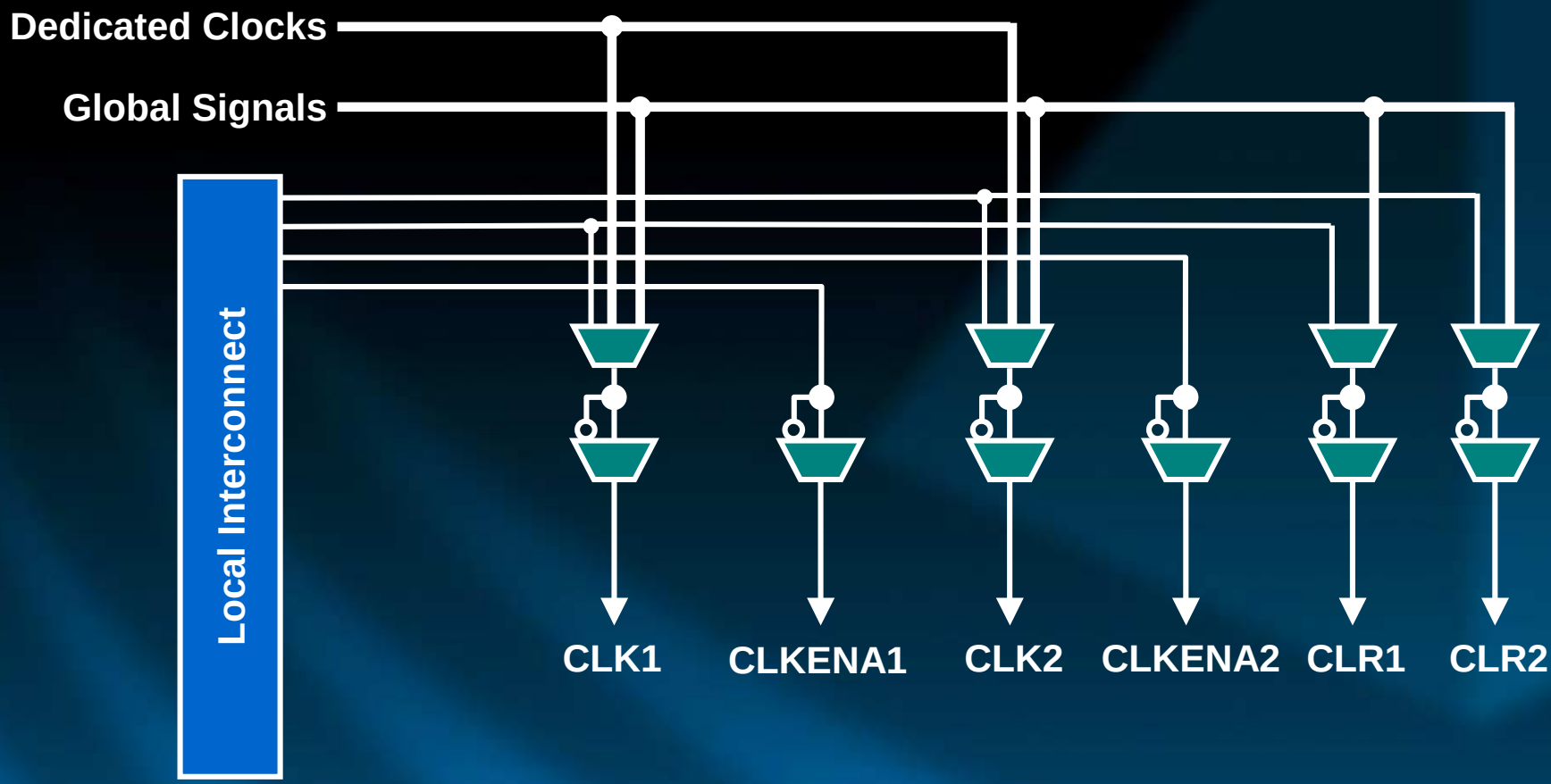
ESB Can Implement Product Terms

- 32 Product Terms per ESB
- 16 Macrocells per ESB
- Each Macrocell Can Expand to the Next
- 1 to 16 Outputs per ESB, Registered Individually
- Benefits
  - Performance
  - Density

Embedded Product-Term Capability



ESB Control Signal Flexibility



Content Addressable Memory (CAM)

- Looks Up Data in Memory & Puts Out Address
- Accelerates Fast Search Applications
  - Functions as a Parallel Comparator
  - Order of Magnitude Faster than RAM (Serial)

Common in High-Speed Communication Applications

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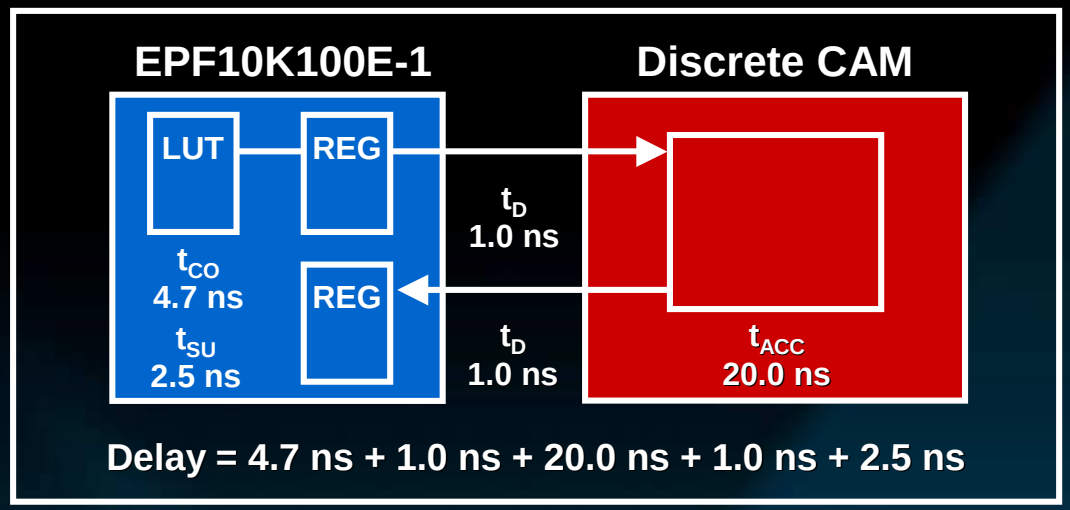
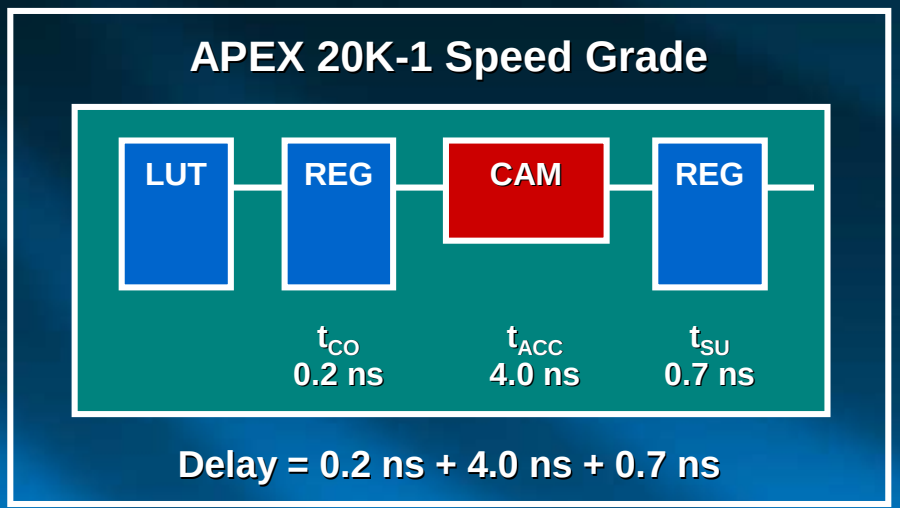
APEX 20K High-Speed CAM

- ESB Supports 1-Kbit CAM
  - 32 Words x 32 Bits
- 4.0-ns Access Time
- Can Cascade ESBs to Build Larger CAMs

CAM Integration Boosts Performance



29.2 ns

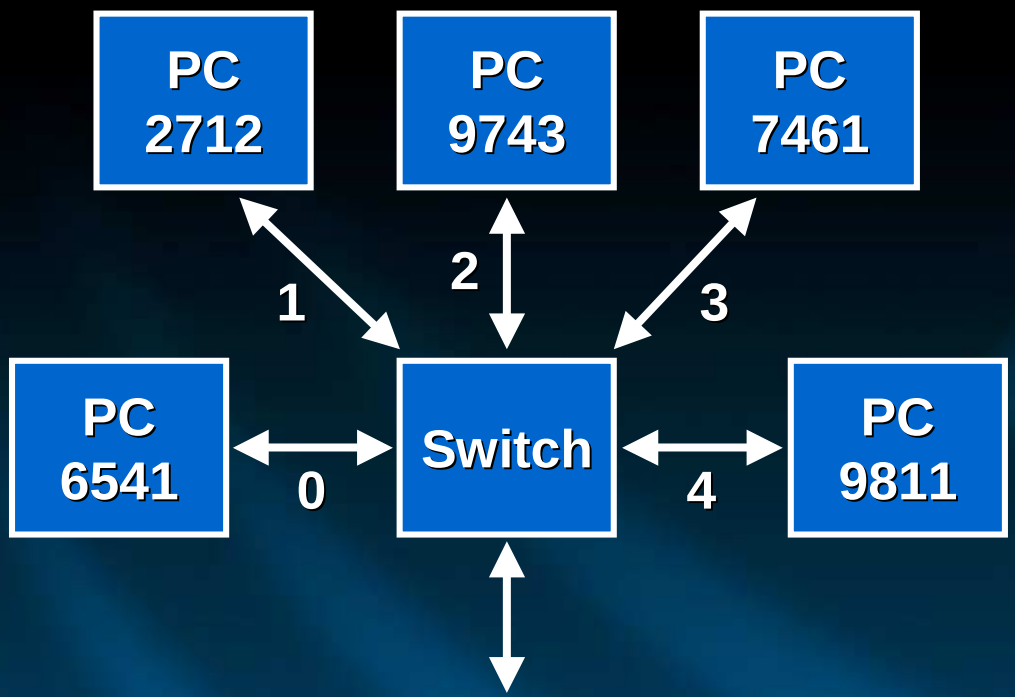


4.9 ns

CAM Applications

- Simple Address Mapping
  - Switch Address Mapping
  - Internal Address Look-up
  - Ethernet Address Look-up
  - ATM Translator
- Pattern Recognition
  - IP Filter
  - Packet Header Identification

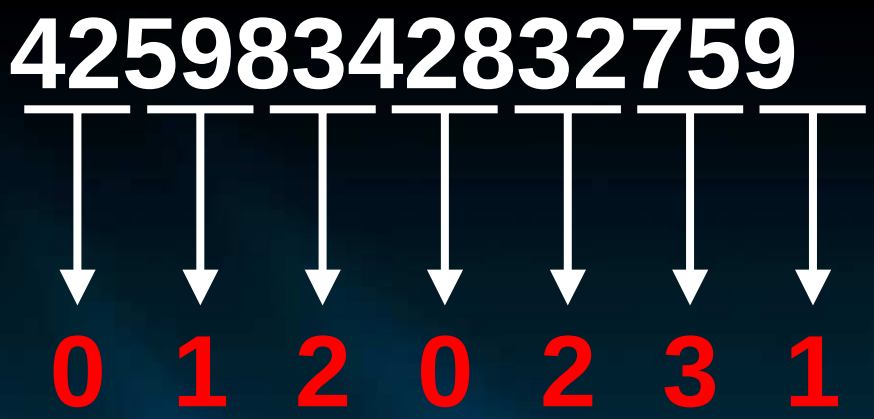
CAM Application: Switch



CAM Contents

Address	Data
0	6541
1	2712
2	9743
3	7461
4	9811

CAM Application: Compression



CAM Contents

Address	Data
0	42
1	59
2	83
3	27

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I/O Pins

- I/O Pins Adjacent to MegaLAB™ Structures
- Local Interconnect Drives I/O Pins
  - Fast t_{CO}
- Row I/O Pins Directly Drive Local Interconnect
  - Fast t_{SU}
- I/O Pins Directly Drive Rows, Columns
  - High Routability
- Individual Tri-State per Pin
  - Locally Driven for Fast Tri-State

MAX

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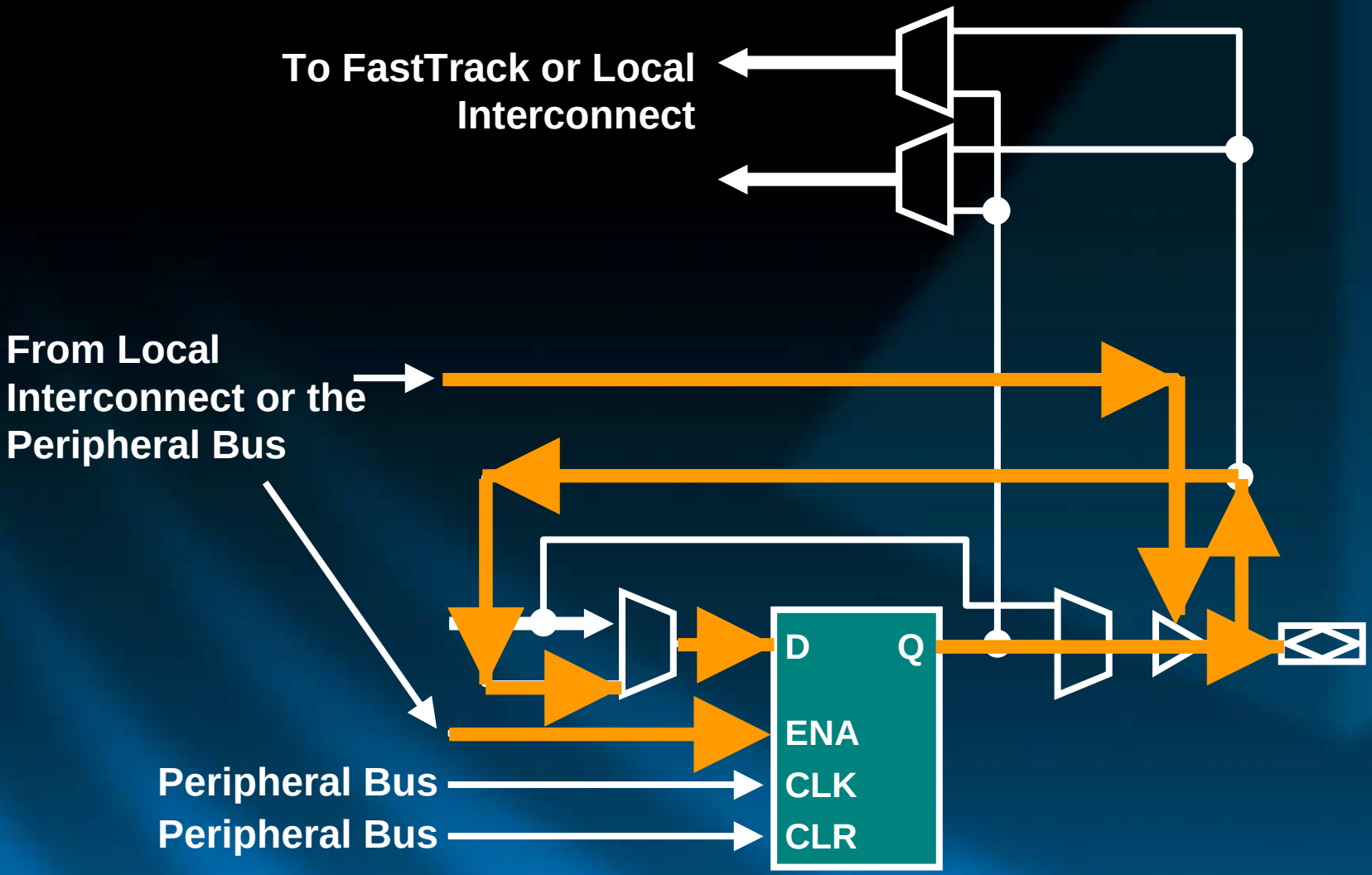
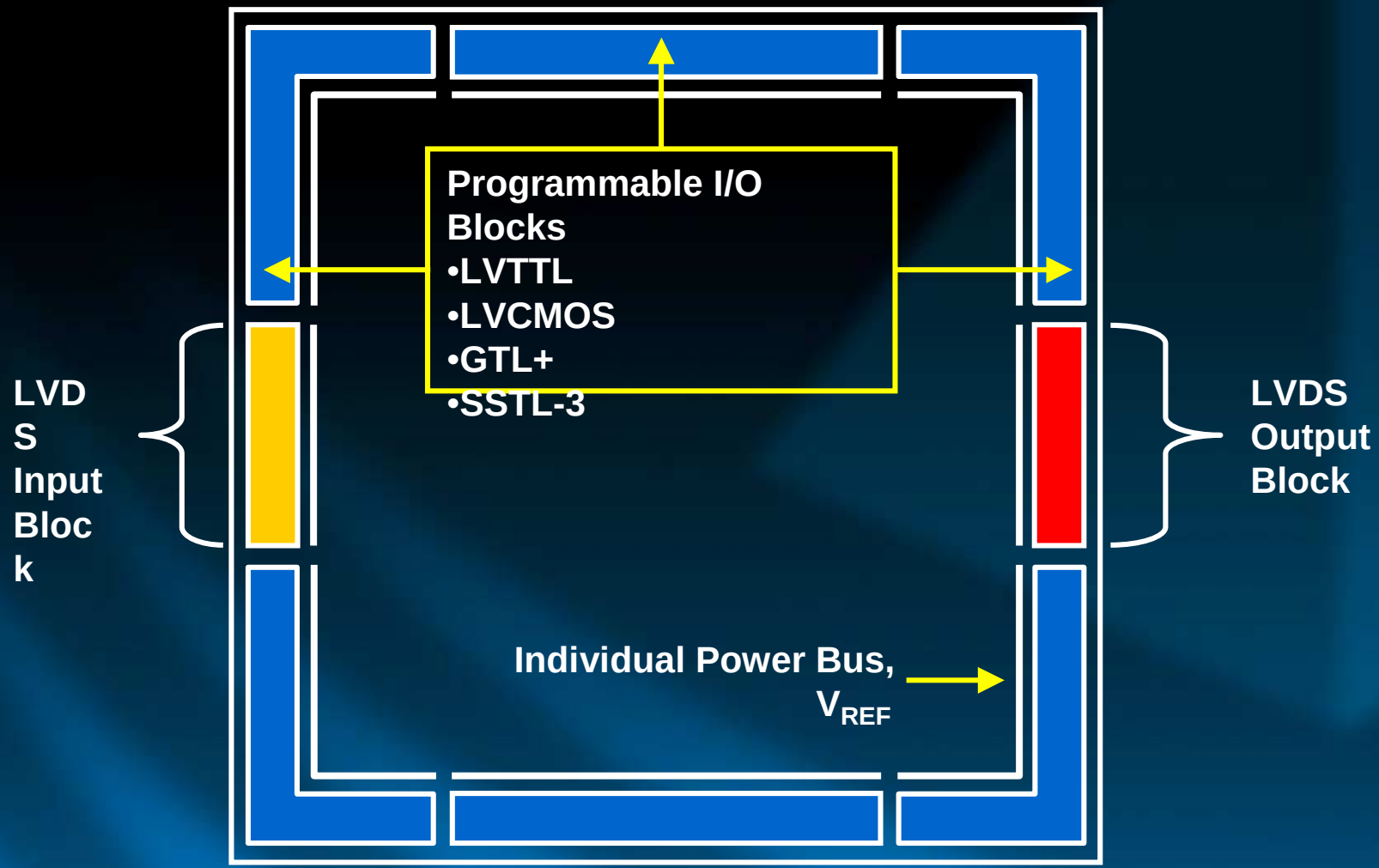
I/O Cell


To FastTrack or Local Interconnect
From Local Interconnect or the Peripheral Bus
Peripheral Bus
Peripheral Bus
D
Q
ENA
CLK
CLR

APEX 20K I/O Features

- Supports Multiple I/O Standards
  - LVTTL, LVCMOS
  - GTL+, CTT, AGP
  - HSTL, SSTL-2, SSTL-3
  - LVDS
- Hot Socketing Support
- MultiVolt™ Support for 1.8-, 2.5-, 3.3-V Devices
- Pin-by-Pin Selectable 3.3-V PCI Clamp

APEX 20KE I/O Blocks



LVDS Characteristics

- Two Pins for Each Signal
  - Differential Determines Value
  - Advantage: Greater Noise Immunity
- Up to 622-Mbps Transfer
- Serial-Parallel Converter at Pin
  - Converts Input Data to 8-Bit Parallel Format
  - Converts Output Data to Serial Format
  - Uses Dedicated PLL

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Preliminary Performance Results

LVDS Mode	Without Deskew	With Deskew	Units
x1	270	N/A	Mbps
x4	1000	Not Required	Mbps
x7	655	672	Mbps
x8	643	660	Mbps

- APEX to APEX Data Transfer
- Room Temp and Typical Voltage

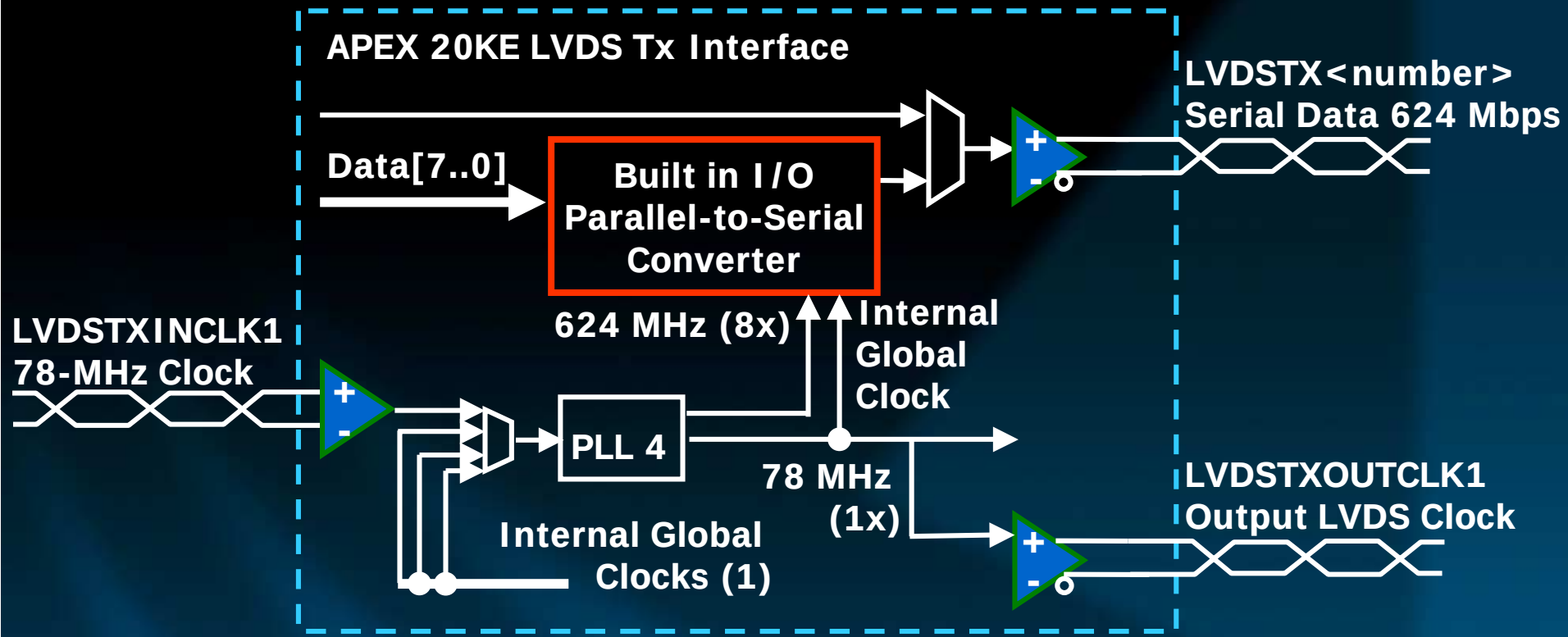
3 Levels of LVDS Support in APEX 20KE

- All APEX 20KE Devices Support LVDS on Clock Pins
  - Dedicated Clocks, Feedback Pins, Output Clock Pins
- EP20K300E Supports LVDS Data in Bypass x1 Mode
- EP20K400E and Larger Support LVDS in all Modes
  - LVDS Clocks and Data in x1 Mode are Supported on non-X Devices
  - x4, x7, x8 Modes are Supported with -X Ordering Code

APEX 20KE LVDS Support

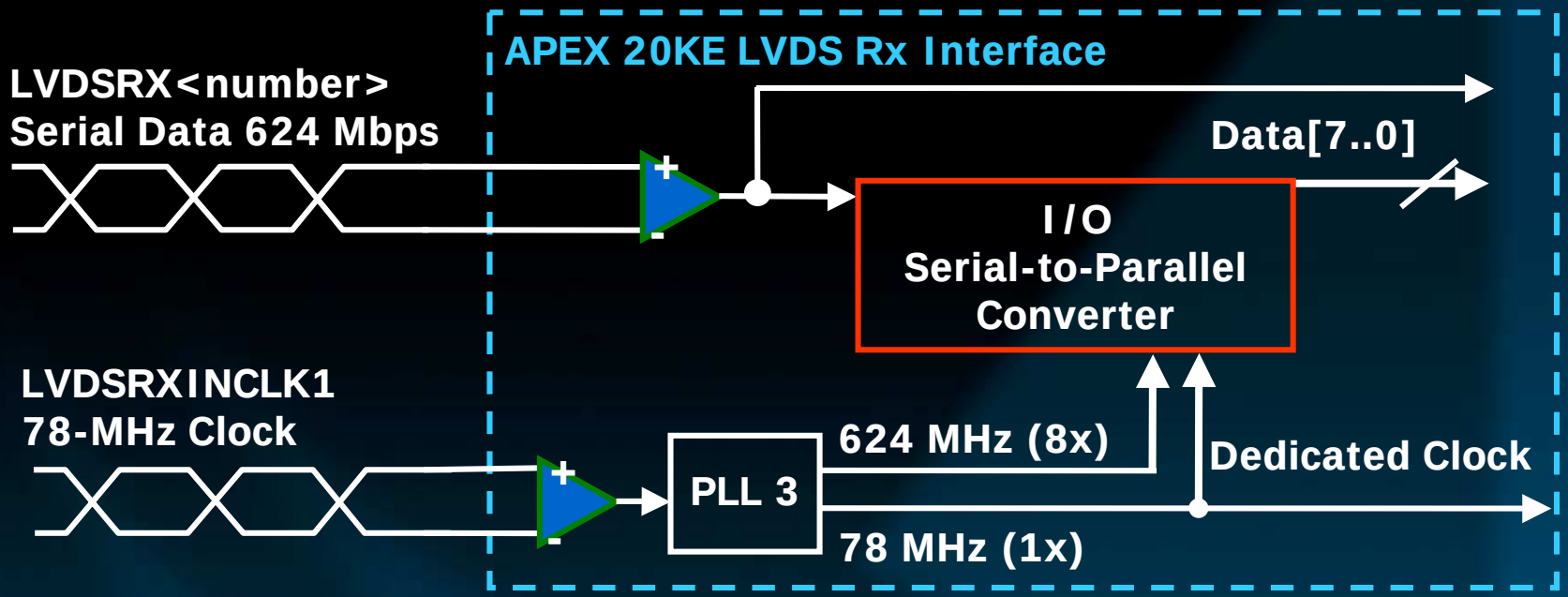
LVDS Mode	<EP20K300E	EP20K300E	>EP20K300E
Clock Pins	✔	✔	✔
x1		✔	✔
x4			-X
x7			-X
x8			-X

LVDS Transmitter Block



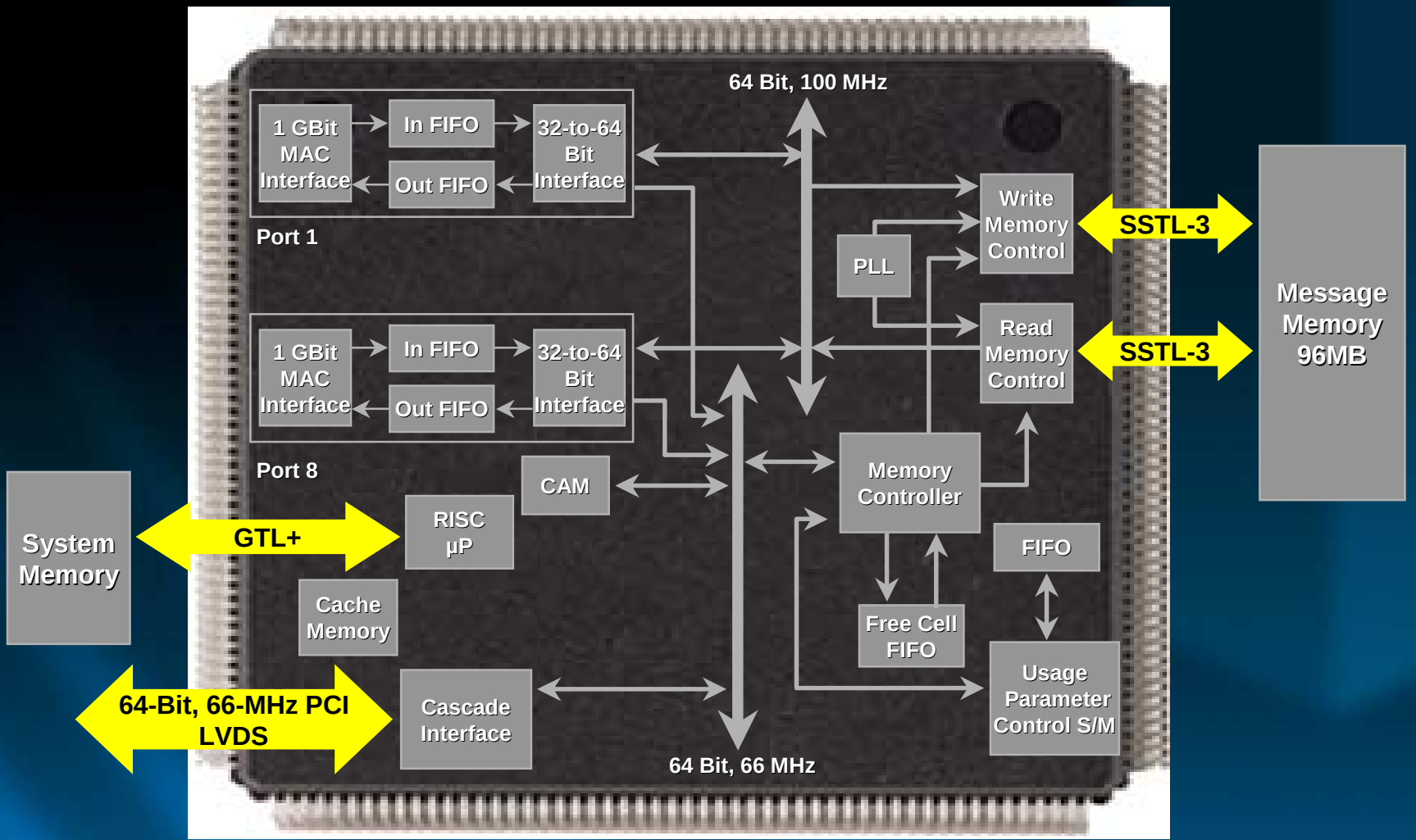
- 16 Transmitter Data Channels Synchronized to 1 Clock
- Optional LVDS Transmitter Input Clock
- Optional Lock and Input Synchronization Clock

LVDS Receiver Block (x8 Mode)



- 16 Receiver Data Channels Synchronized to 1 clock
- Optional Deskew and Lock pins

Complete Interfacing Solution



APEX 20K ClockLock, ClockBoost

- ClockLock™ Synchronization Circuitry
- ClockBoost™ Multiplication Circuitry (2X, 4X)
- 25-133 MHz Range
- 250-ps Jitter

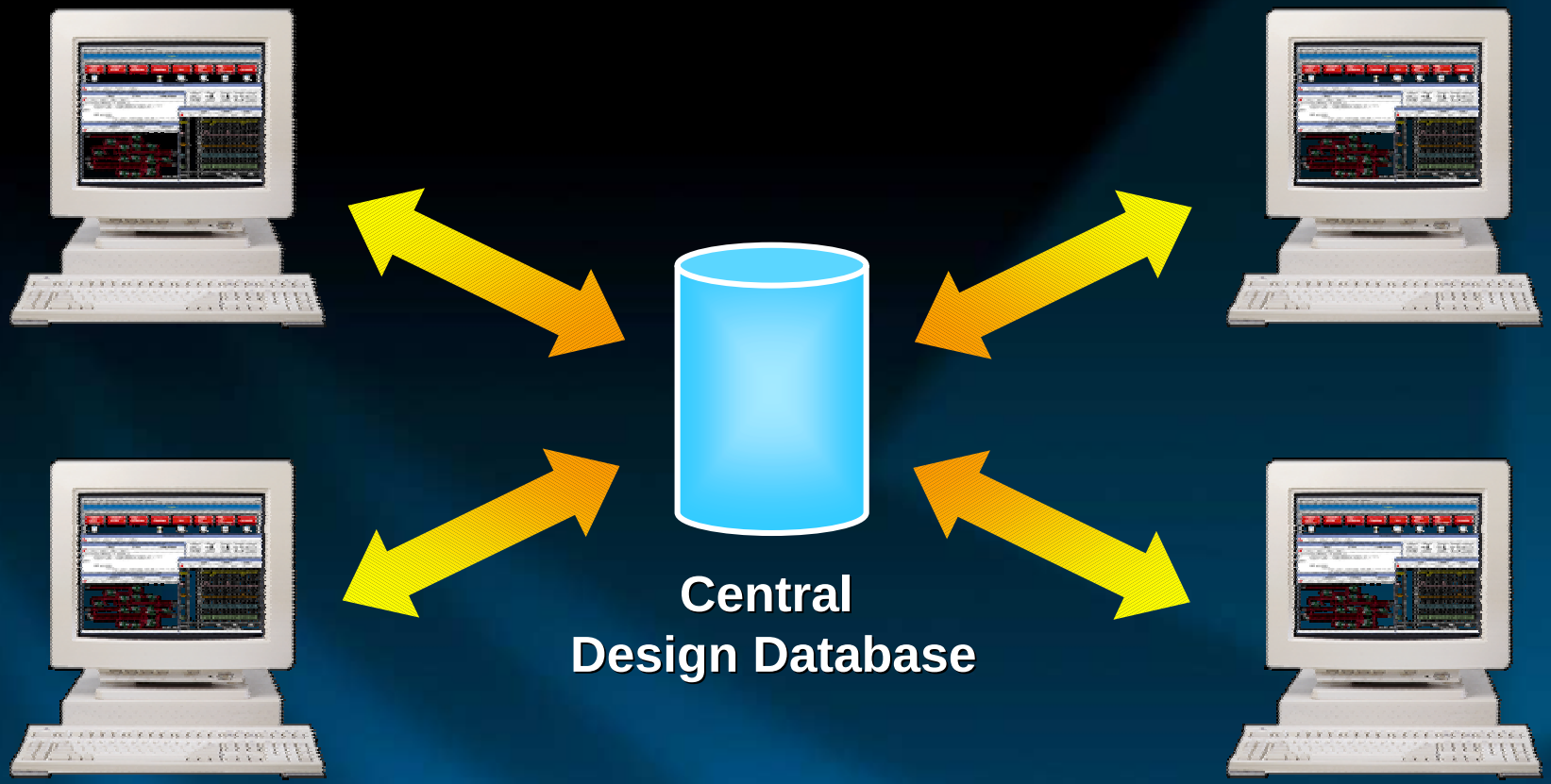
APEX 20KE ClockLock, ClockBoost

- Four PLLs
  - Two for LVDS or General-Purpose, User Selectable
  - Two General-Purpose
- Frequency Range
  - Input Frequency: 1-160 MHz (Depending on Multiplication)
  - Output Frequency: 20-200 MHz

APEX 20KE ClockLock, ClockBoost

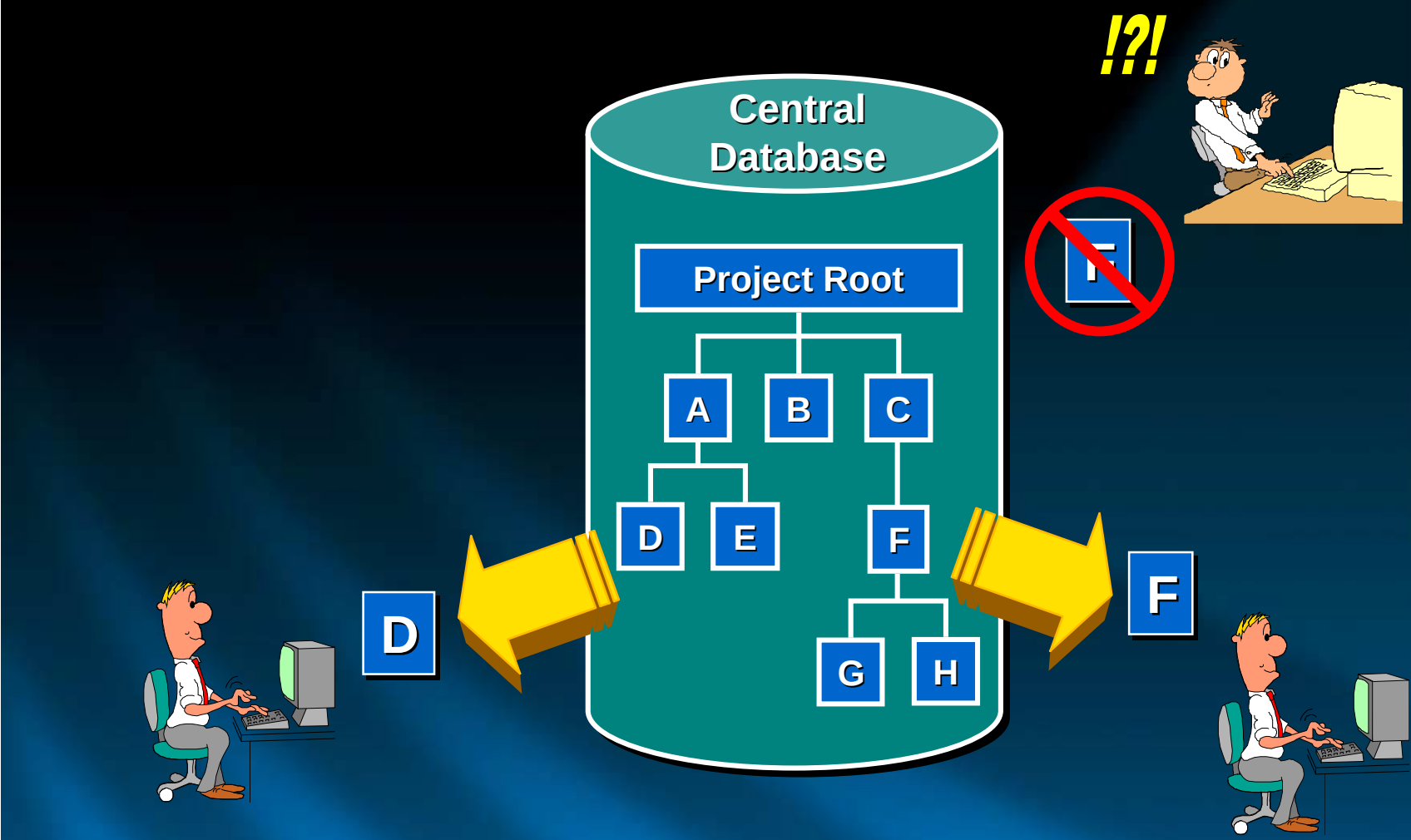
- Multiplication
  - Supports m/n Multiplication
    - m=1-16, n=1-256
  - Supports 1.544 to 2.048 Conversion (T1/E1)
- Phase Adjustment
  - ±2 ns Linear Shift (0.5-ns Precision)
  - 90º, 180º, 270º Phase Shift
- Drive PLL Output Off-Chip

Workgroup-Based Design

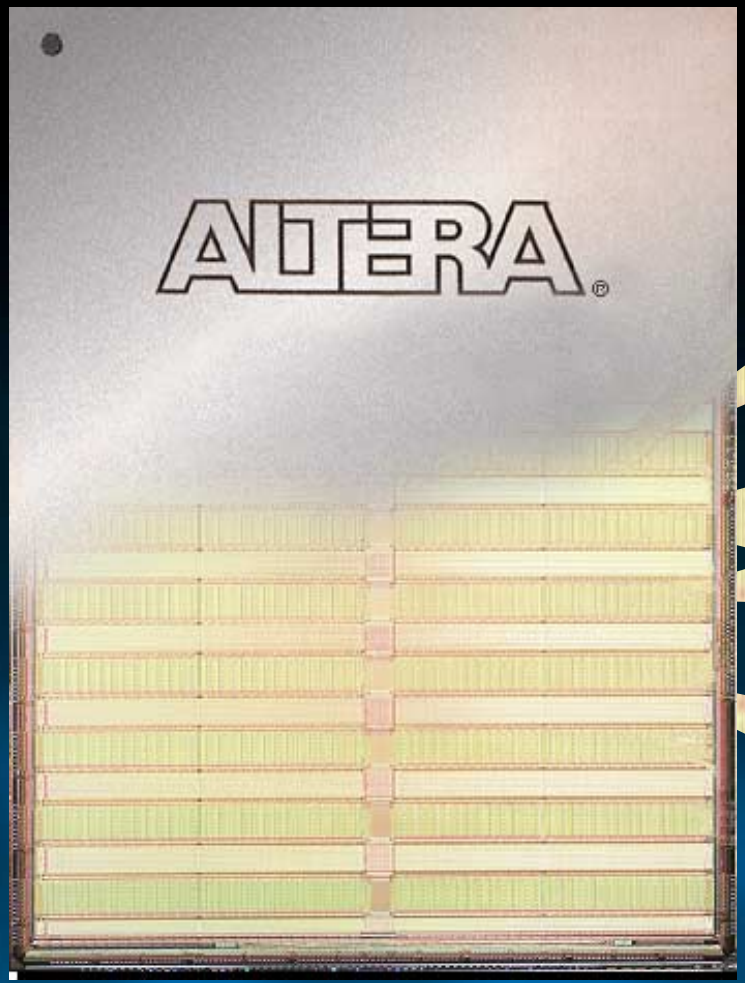


Design Revision Control
Global File Management

Shared Work Environment



Row-Based Multi-Processor Computing



Single Pentium System

CPU

Dual Pentium System

CPU 1

CPU 2

SPARCSTATION

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Design Integration

- MultiCore™ Allows Different Kinds of Logic
- Programmable I/Os Interface with Other Chips
- ClockLock, ClockBoost PLLs for Tuning Timing
- Workgroup Computing Allows Design Teams
- Multi-Processor Support Allows Fitting on Multiple Computers