Altera Technical Solutions Seminar 2000

MJL

ALTERA®

Schedule

- Opening
- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo

Agenda

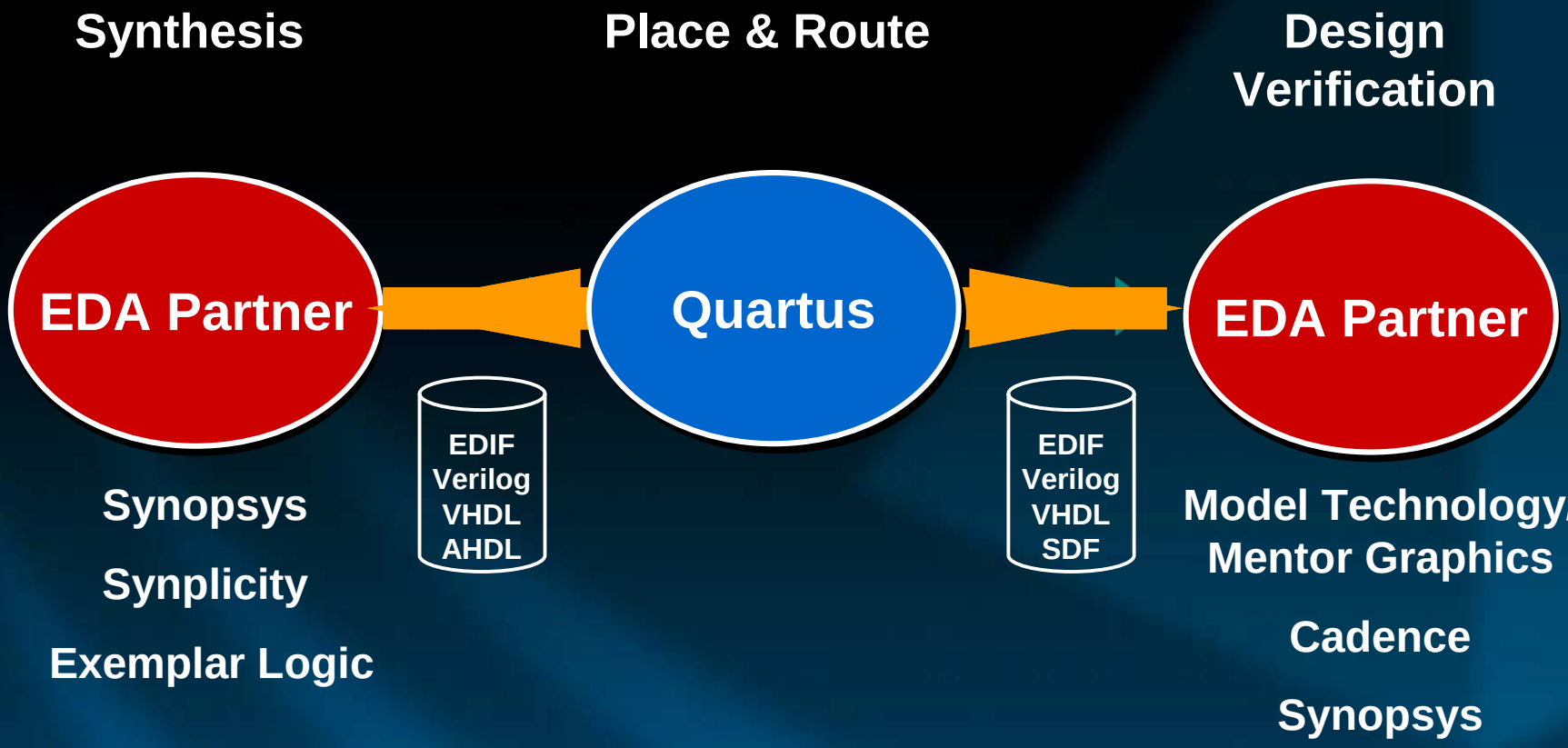
- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap

- NativeLink™ Integration
- Scripting

MDL

ALTERA®

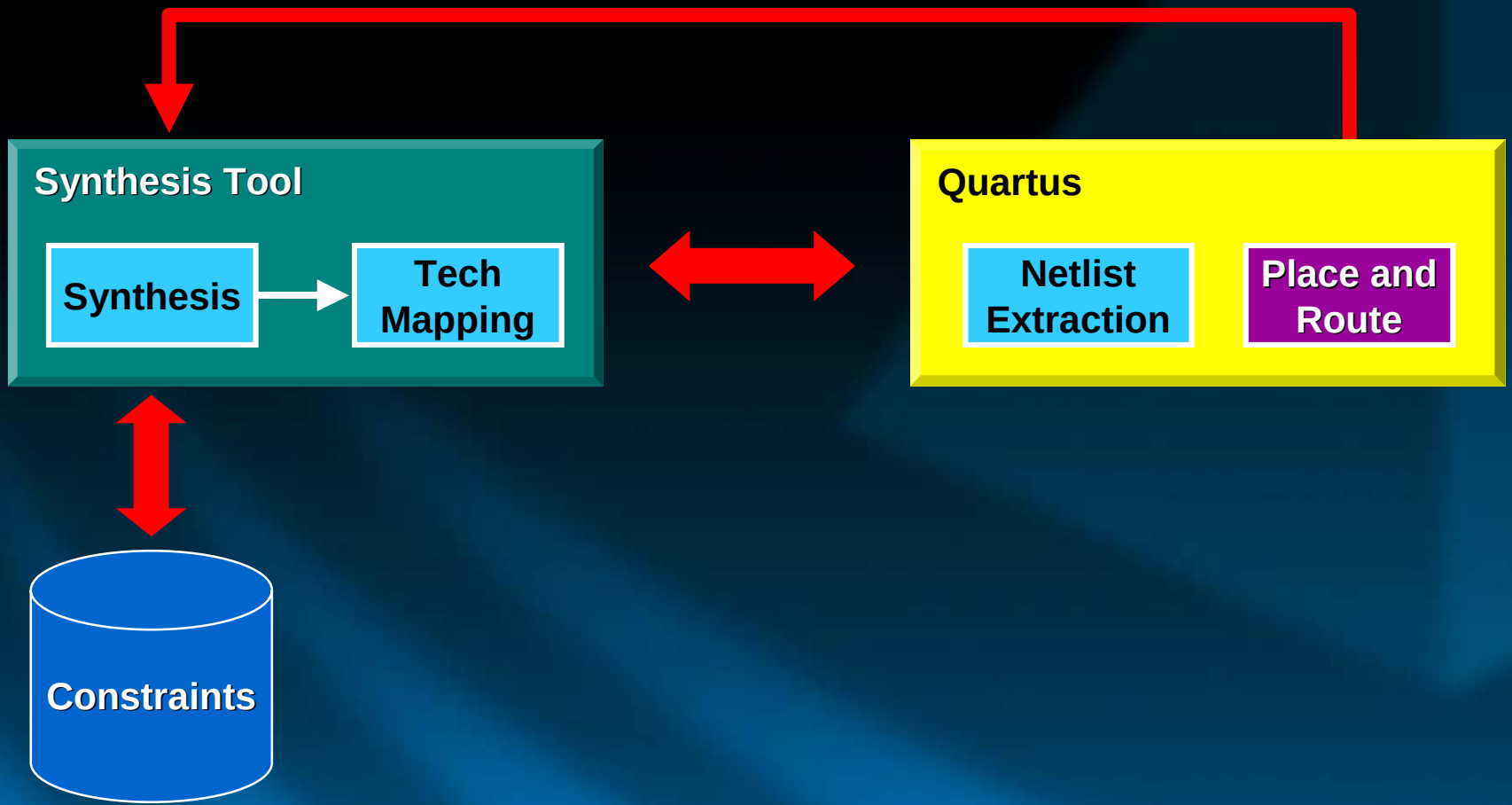
Integration with EDA Partners



NativeLink EDA Integration

- Seamless Interfaces with Popular Tools
  - EDA Tools Can Run Seamlessly in Quartus
  - Quartus Can Run Seamlessly in EDA Tools
- Improved Utilization and Timing Prediction Available for Synthesis Tools
  - Run-Time Access to Quartus Device and Project Databases

Adaptive Timing-Driven Synthesis



Scripting Capabilities

- Two Powerful Scripting Languages
  - Visual Basic
  - TCL/TK (Platform Independent)
- Total Automation
  - A Single Script Can Run an EDA Tool and Quartus
  - Customize Output to Suit Specific Needs
  - Customize Input Settings in a Spreadsheet or Text File

ModelSim PE - Highlights

- 100% VHDL,Verilog Support
  - Supported on all Platforms (98, NT, Solaris, HP)
    - Testbench Support
    - “Behavioral” Constructs Support
- HDL Debugging Environment
  - HDL Compiler, Simulator, Source Editor, Waveform viewer, Dataflow Manager
- Optimized Direct Compiled Architecture
  - Compiles HDL directly to machine independent object code
- Tcl Scripting Support
- Integration w/ other EDA tools in the industry
  - Quartus, MP2, Renoir, Leonardo Spectrum etc.

FPGA *Express* Features

- Architecture-specific mapping for high QoR
  - ATOMs (I/O, Lcell, etc.)
  - Carry/cascade chains
- LPM inferencing
  - Multiplier LPMs inferred for FLEX and APEX devices
  - Other arithmetic operators are implemented using ATOMs and carry chains
- Automatic Global Signal Mapping

FPGA *Express* Features

- TimeTracker
  - Spreadsheet-based timing analysis tool
  - Saves time by catching timing issues before P&R
- VisTA Schematic Viewer
  - Tightly linked with TimeTracker for graphical analysis
  - Analyze RTL and optimized design schematics
- Easy-to-use Synthesis Control
  - Push-button flow
  - Constraint-based flow
  - Hierarchical flow
  - Script-based flow

MJL

ALTERA®

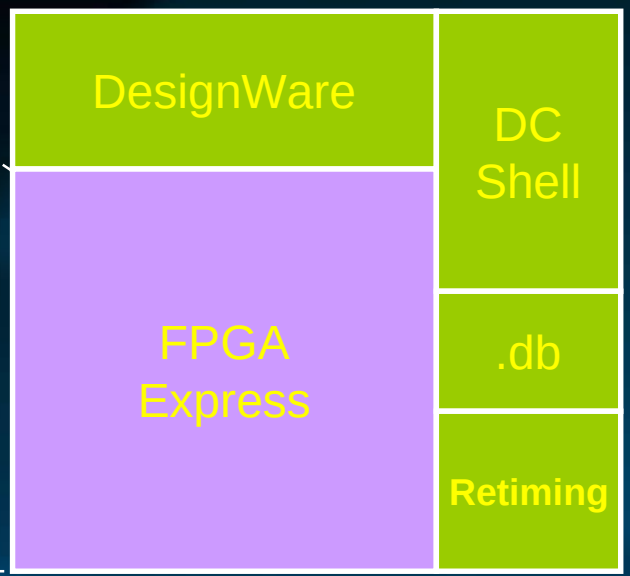
FPGA Express Vs FPGA Compiler II

- **What is FPGA Compiler II Altera Edition ?**

FPGA Express

- Push-Button Flow
- Industry-Standard HDL Support
- Built-In Static Timing Analysis Tool
- Schematic Viewer
- Integration with MAX+plus II & Quartus

FPGA Compiler II (Altera Edition)



FPGA Compiler II - Altera Edition

- Superset of FPGA *Express* Plus...
- Design Ware Support:
  - FC II Altera edition supports the DesignWare™ Foundation components.
  - Instantiated DesignWare components are synthesized using FC II with no user intervention.
  - FCII Does not infer DesignWare components,
    - Uses a Built-in module generator to infer the optimal operator.
- .db File Support:
  - FCII can export a DB File to Primetime or DC or Formality

MJL

ALTERA®

FPGA Compiler II - Altera Edition

- DC Shell Script translation
  - Helps easy ASIC -> FPGA Migration:
  - Most DC users utilize the scripting capability to automate their design flow.
  - Utility to help these designers migrate to FC II
    - fc2_altera_shell > translate_dc_script –input_script *dc_shell.scr* –output_script *fc2.scr*
      - where dc_shell.scr is the original dc_shell script and fc2.scr is the translated script.

- All GUI Actions in FCII have an Equivalent shell command

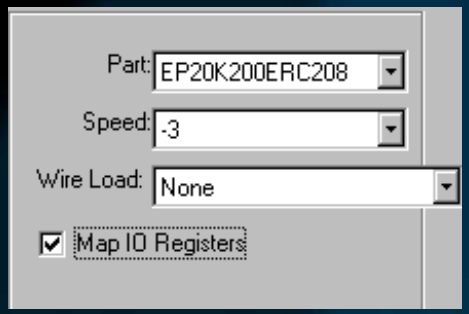
Leonardo Spectrum Update

- Device Support Update:
  - 1999.1h: MAX 7000 A/E/S Support
  - 1999.1i: MAX 3000 Support
  - 2000.1: ACEX Support (in the April time frame)

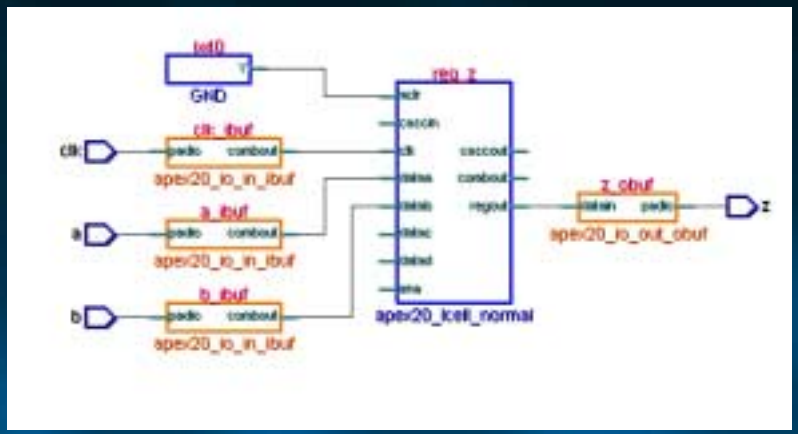
exemplar

Leonardo Spectrum Update

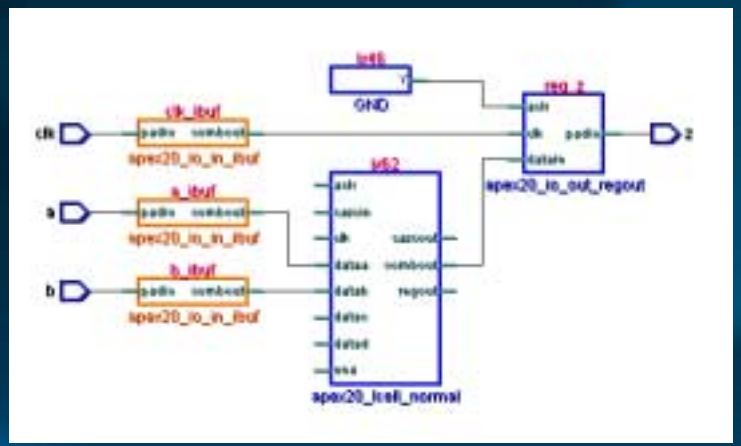
Technology Form



- **1999.1 I/O Register Packing:**
  - **Default to OFF**
  - **Set from the Technology Form**
  - **Will Bring Internal Flops into the I/O ATOMs**



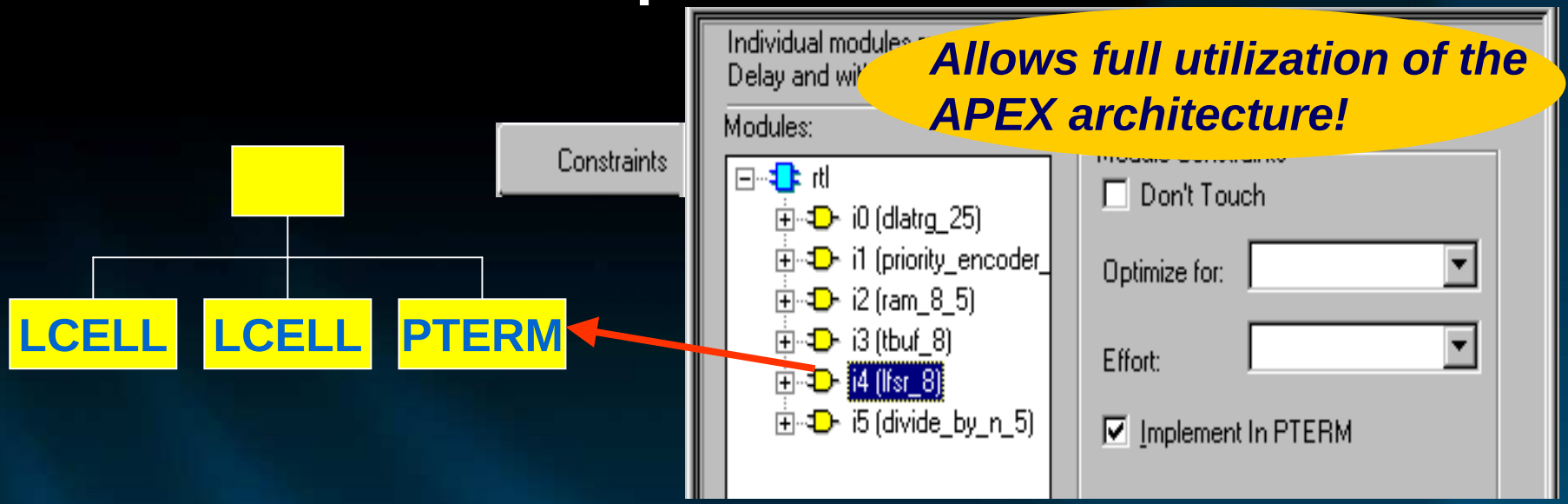
Unpacked



Packed

Leonardo Spectrum Update

- 1999.1i: PTERM Optimization for APEX



- PTERM Constraint Set on Instance
- Implemented as Sum-of-Products Logic
- Quartus Instructed to Implement in PTERMs through Native-Link (passed as Tcl Constraint)

MJL

ALTERA

Leonardo Spectrum Update

- Coming in 2000.1a
  - Beta in March 2000
  - Production in April 2000
  - New Schematic Viewer (Leonardo Insight)
  - Integrated Design Browser
- Also coming in 2000
  - In-Place Optimization Flow
    - Re-optimize critical paths after place and route
    - Optimize the “real critical paths “
    - Reduce design iterations through place and route

MJL

ALTERA®

Benchmark Score (23 designs,win point)

FC2 : Synplify : Leonardo

	f_{MAX}	Area	Time
TDC Off	4:14:5	1:9:13	3:8:12
TDC On	3:13:7	1:10:12	5:7:11

EDA Integration Summary

- Quartus Fits Seamlessly into Existing Flows
  - Can Work Under the Command of Other Tools
  - Can Launch Other Tools and Vice Versa
- Tools Can Communicate with Each Other
  - Constraints and Results Can Be Passed Between Tools
- CAD Managers Can Script Custom Flows