Altera Technical Solutions Seminar 2000

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Schedule

- Opening
- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo

Agenda

- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- **Intellectual Property**
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap

The SOPC Solutions Program

- Objective
  - To provide the field with compiled sales and technical collateral for SOPC
  - Bridge Between Systems and IP Info
- Approach
  - Three Specific Application Examples
  - Each Solution Highlights IP and APEX Features
  - Megacore/AMPP Agnostic –Relevant IP Will be Included

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Sources of Altera IP Cores

- Broad range of Megafunctions
- Sourced by IP Partners
- Consulting Services Available
- Source Code Licenses Available

AMPP
ALTERA MEGAFUNCTION PARTNERS PROGRAM

- Sourced by Altera
- Focused Set of Standard Functions

MegaCore

Quoted by AMPP Partners Directly

Quoted by Altera Sales directly

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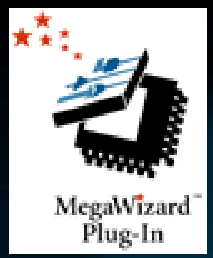
IP Integration Flow

OpenCore™ Download

Free

Free

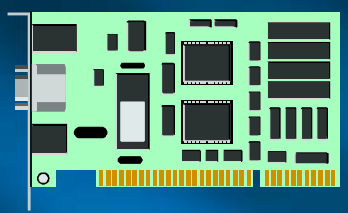
MegaWizard Parameterization

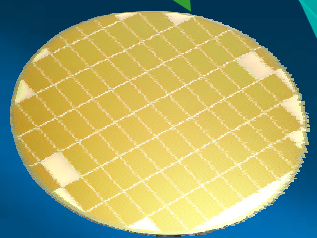


MAX+PLUS® II and
Quartus™ Software

Customer Pays for License to Write POF

Silicon &
Development Board





Obtain

Modify

Analyze

License

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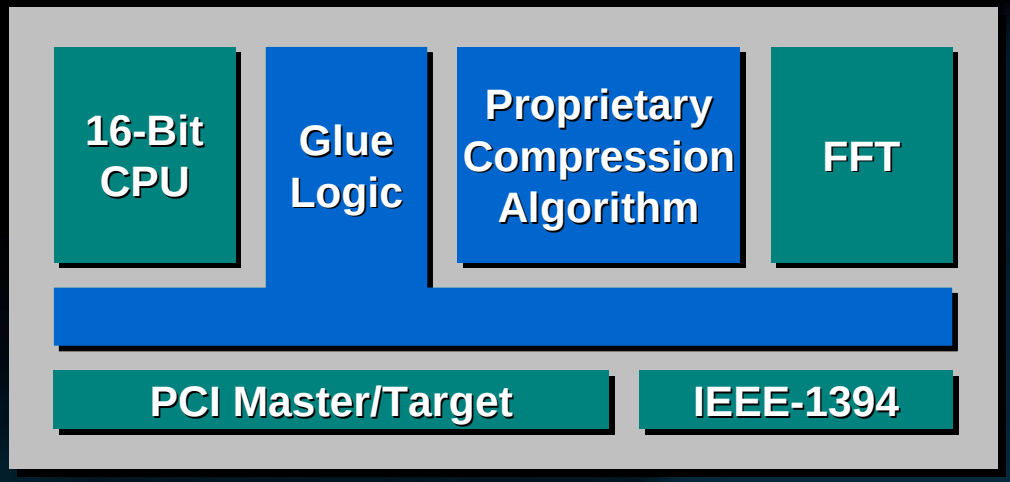
Concentrate on Adding Value



Standard Design Blocks
- Best Performance
- Proven Solution
- Fast Implementation/ Integration

Proprietary Design Blocks
- Innovative
- High Value Added

- ***Focus on the High-Value, Proprietary Functions***
- ***Use Megafunctions for Common, Standard Functions***

MegaCore™ & AMPP℠ Functions Offered

- Processors and Peripherals
- PCI and Bus Interfaces
- DSP and Communications
- Networking

100+ Available AMPP Cores...

ALTERA MEGAFUNCTION PARTNERS PROGRAM

IEEE 1284 Parallel Interface
IEEE 1394a Link Layer Ctrl
10/100 Fast Ethernet MAC
2910, 2910A Controllers
29116A 16-Bit Processor
49410 Controller
68450 DMA Controller
6850 ACIA
8255A Interface
16450/16550 UART
32-bit Microprocessor
6502 Processor
Z80 Processor
8031/8051 Processors
8032/8052 Processors
Adaptive Filters
Bit Error Rate Tester

Complex Mixer/Multiplier
Convolutional Interleaver
Decimating Filter
Digital Modulator
Digital Data Acquisition Function
DVB FEC Subsystem
Discrete Cosine Transform
FFT/IFFT
FIR Filter
HDLC
IIC Master and Slave
IIR Filter Library
Image Processing Library
Linear Feedback Shift Register
Multi-Standard ADPCM
MIPS Class Processor
Numerically Controlled Oscillator
Packet over SONET Controller

PCI Master/Target (3 Partners)
PCI-PowerPC Bridge
PowerPC Bus Arbiter
PowerPC Bus Master
PowerPC Bus Slave
Reed-Solomon Decoder
Reed-Solomon Encoder
RISC Processor
SDRAM Controllers (3 Partners)
SONET Byte Bus I/F
Speedbridge FIFO
Symbol Interleaver
Telephony Tone Generation
USB Function Controller
USB Host Controller
UTOPIA 2 Master/Slaves

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...From 28 Current AMPP Partners

Northwest Logic Design

tensilica

Applied MICROELECTRONICS

DCM DATA SYSTEMS

PALMCHIP

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Selected New AMPP Cores In 1999

- 100 MHz SDRAM Controller
- UTOPIA II Master Slave/ Receive Transmit
- Gigabit Ethernet MAC
- 1394 Link Layer Controller
- 64-bit/66 MHz PCI Master/Target
- Digital Data Acquisition Function
- CRC10, CRC32 for ATM Systems
- DVB FEC Subsystem
- RISC Processor
- Packet over SONET Controller
- ATM Receive Processor
- Bit Error Rate Tester
- Sony/Philips Digital Interface for Audio
- V8086 Microprocessor

More to be Announced!

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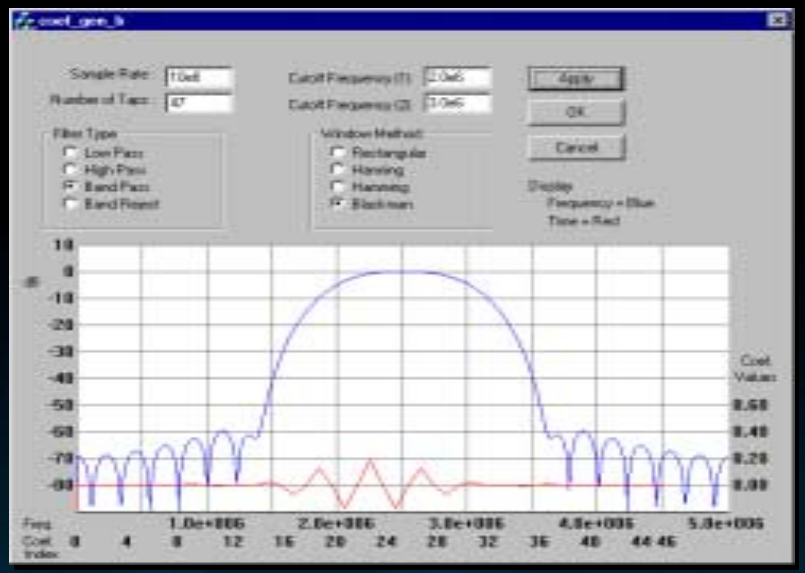
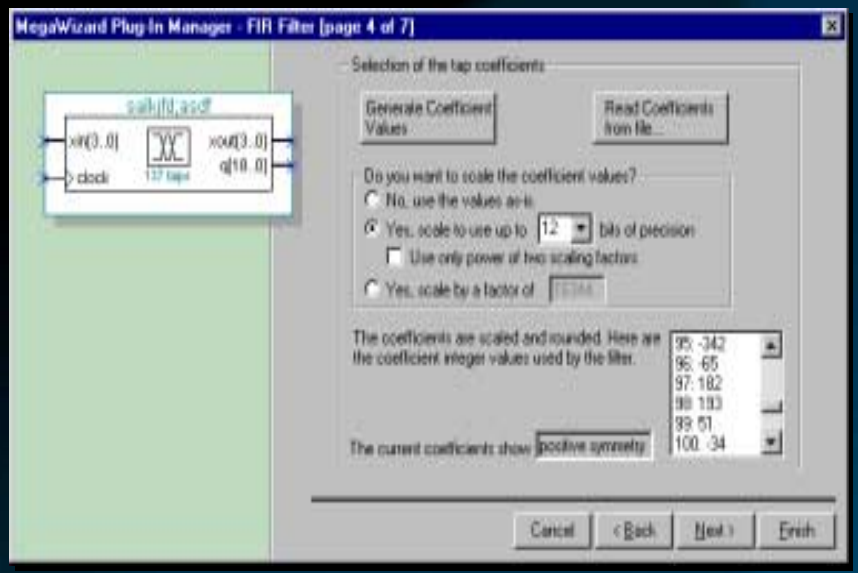
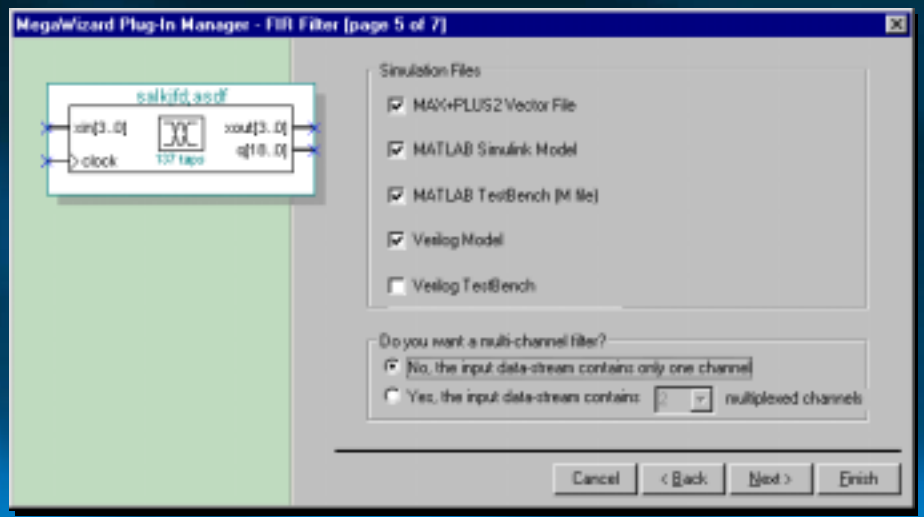
FIR Filter Compiler MegaWizard™ Plug-In







Efficient Megafunction Integration

Megafunction	EP20K400	EP20K1000E
Gigabit Ethernet MAC Interface (x8)	23%	9%
RISC ✪Processor	28%	11%
64-Bit, 66-MHz PCI Megafunction	5%	2%

Reed-Solomon Compiler

- Fully Parameterised Reed-Solomon codes
- Flexible licensing - only buy required features
- Reed-Solomon Compiler 1 (December, 1999)
  - Standard encoder
  - Standard decoder (discrete and streaming)
    - Erasure support option
- Reed-Solomon Compiler 2 (February, 2000)
  - Adds variable encoder
  - Adds continuous decoder (with erasure support option)
  - Adds variable decoder option for standard decoder

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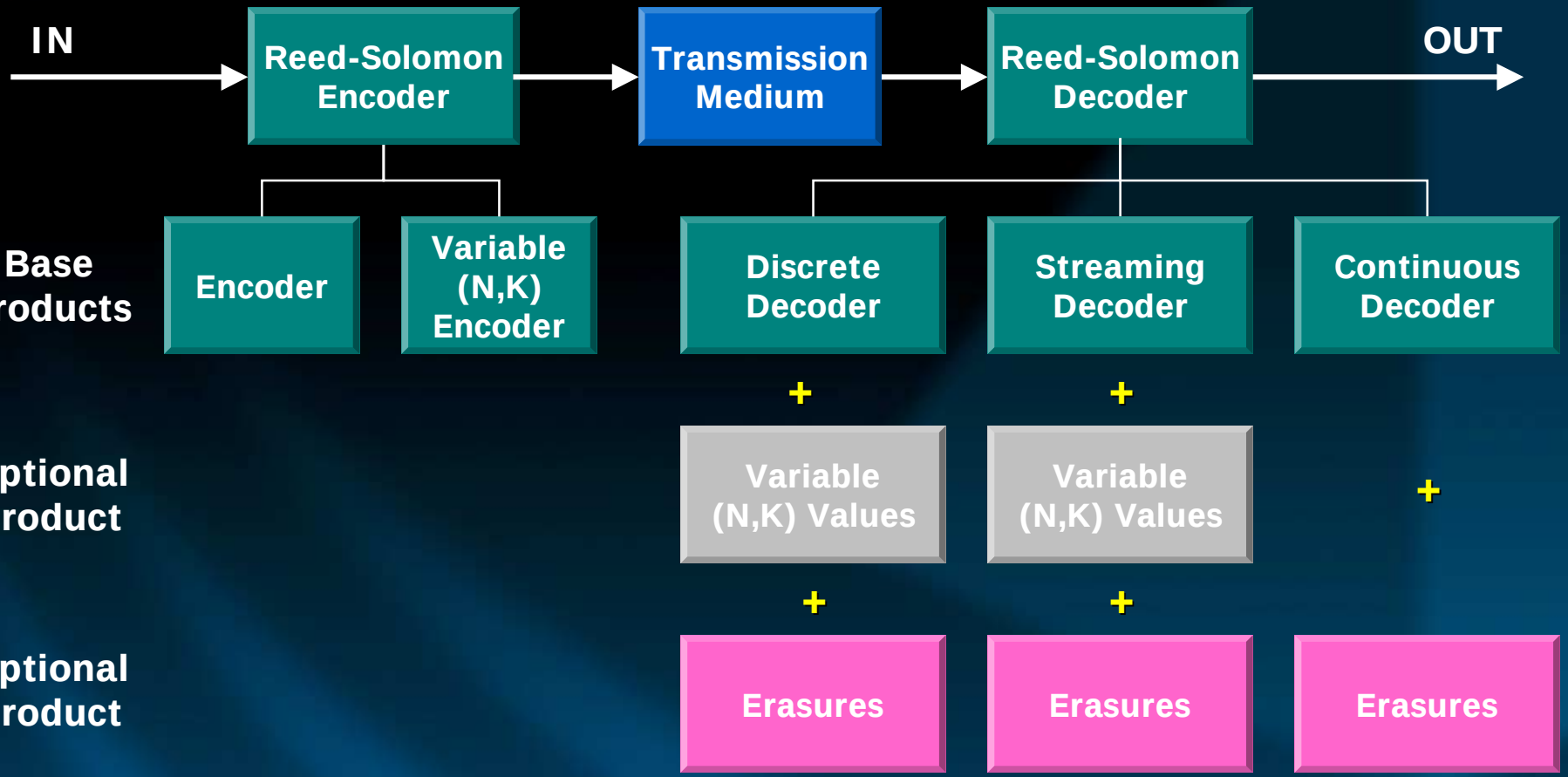
Reed Solomon - Configuration Options



Reed Solomon Compiler 2.0 Supports all these options

Viterbi Decoder MegaCore Functions

- High Speed Parallel
  - Pure Logic Implementation
  - Performance : over 100 Mb/s
  - Fully Parallel Operation
  - Hard Decision and Soft Decision
- Hybrid Serial/Parallel
  - Mixed Serial / Parallel Implementation
  - Typical Performance : 1-8 Mb/s
  - Medium Logic area
- Low Speed Serial
  - Memory based architecture
  - Typical performance : 500kb/s - 3Mb/s

Performance

- Performance of different architectures

	CONSTRAINT LENGTH = 5	CONSTRAINT LENGTH = 7	CONSTRAINT LENGTH = 9
SERIAL	500 LEs	700 LEs	1300 LEs
	3Mb/s	2Mb/s	500kb/s
SERIAL/PARALLEL		1300 LEs	2600 LEs
		8Mb/s	2Mb/s
PARALLEL	1500 LEs	7500 LEs	
	100+Mb/s	100Mb/s	

Turbo Codec MegaCore Functions

- Turbo Codec for 3rd Generation Wireless - March 2000
  - Optimised for APEX 20K
  - Separate Encoder and Decoder Cores
  - Can achieve 2 Mbps
  - Fully Compliant with latest 3GPP Specifications
    - We will update to specifications if they change
  - Includes Algorithmic 3GPP Compliant Interleaver
    - *This is hard to implement and is a key selling feature*
- Turbo Compiler - Q4 2000
  - General Purpose Parameterised Core
  - Support for Higher Bit Rates

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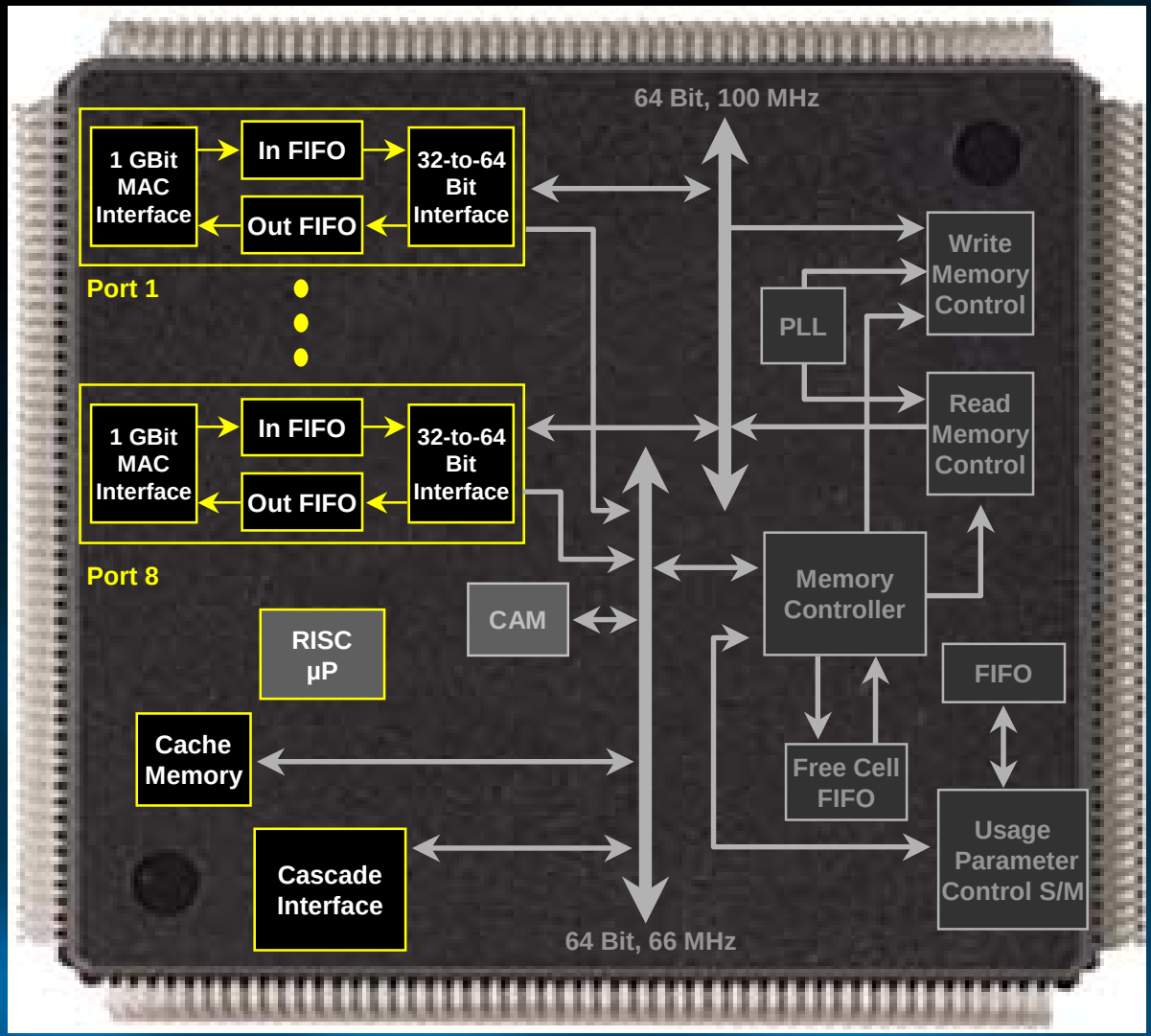
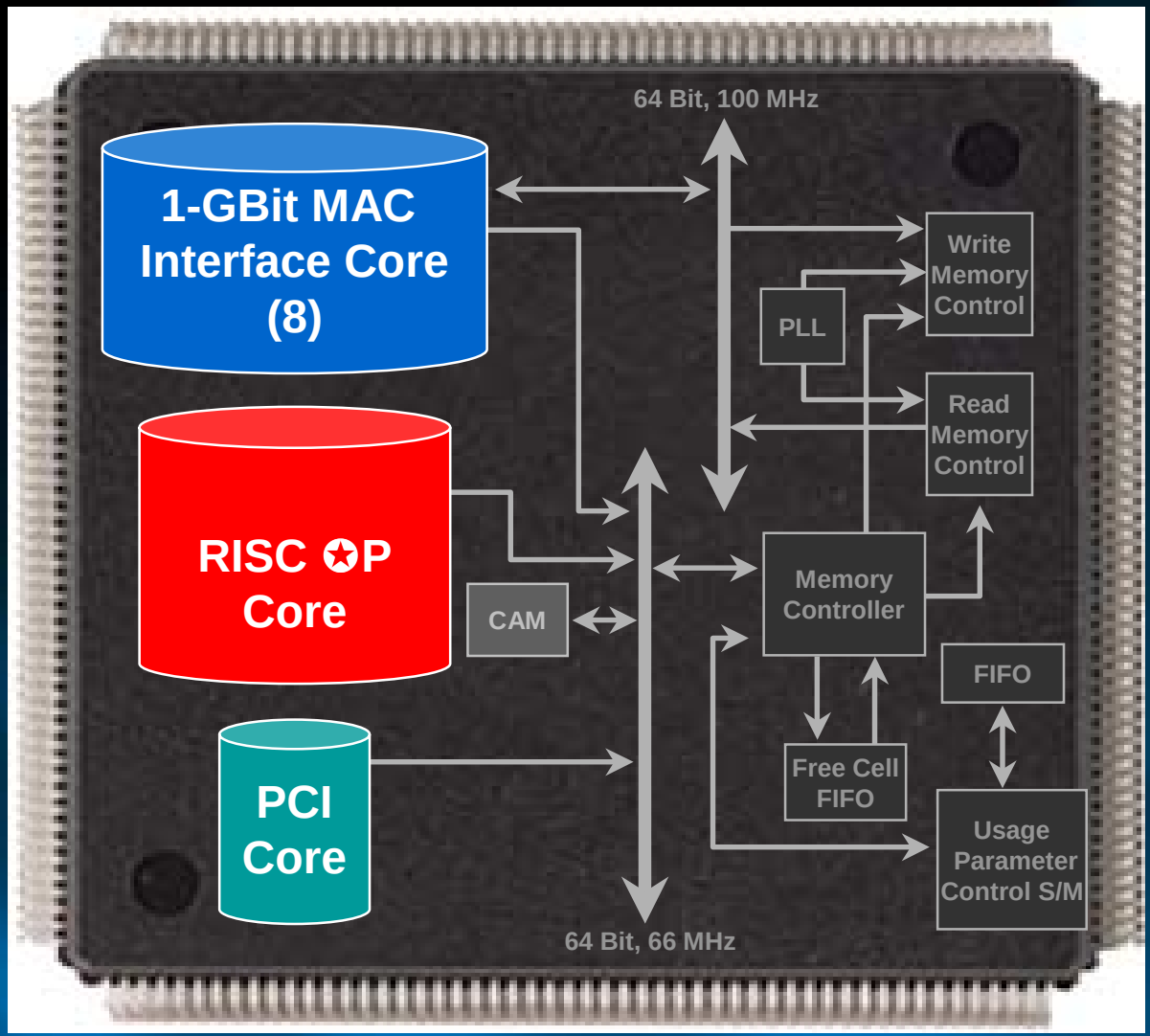
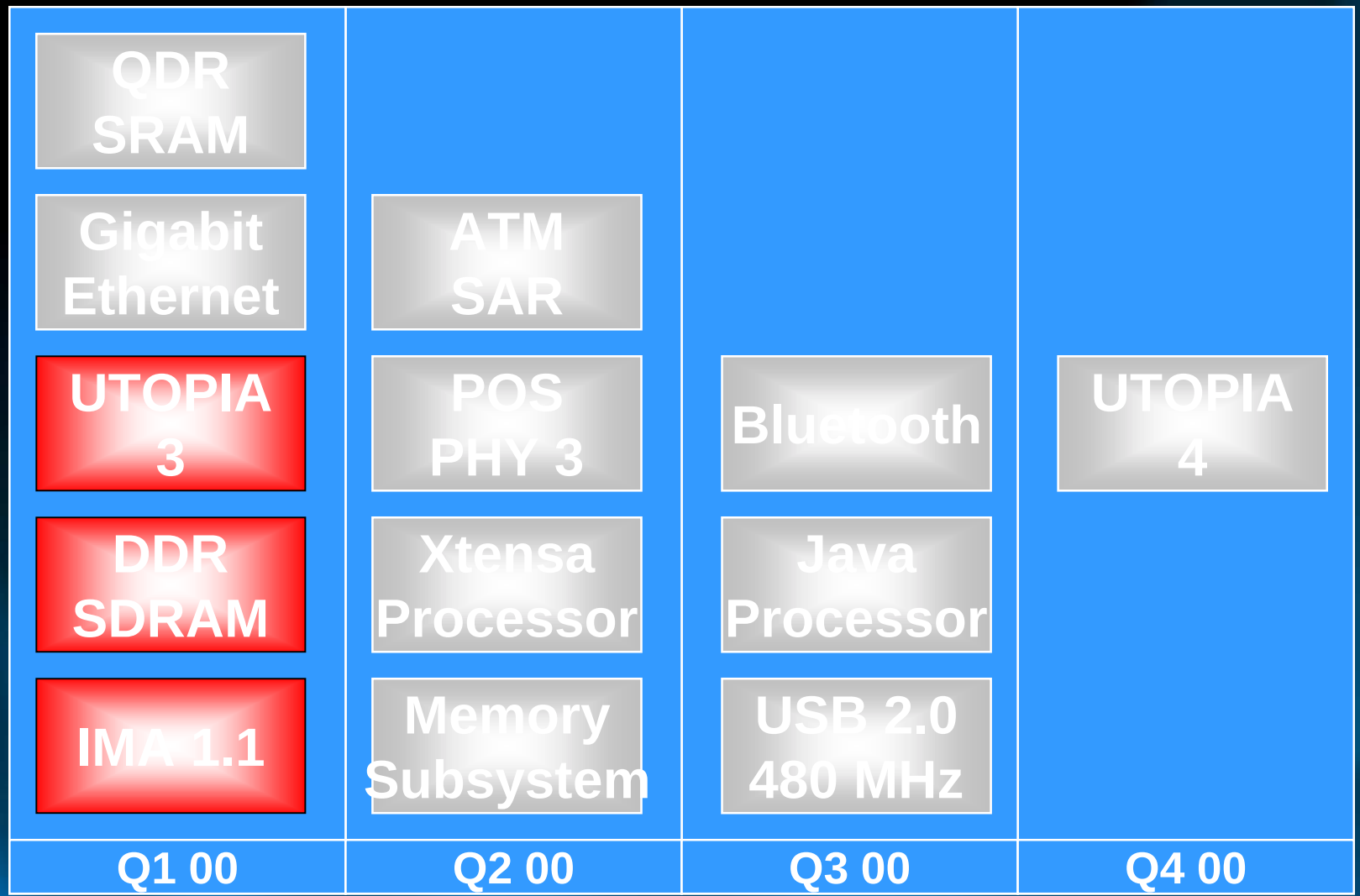
Ethernet Example



Ethernet Example



AMPP Integrated Roadmap 2000



Where Altera is Ahead with Partners

Core Type	Altera	Xilinx
PCI-X	DCM Technologies MegaCore	None
32-bit Processors	Tensilica ARC Cores Lexra	None
Gigabit Ethernet	SRTI CoreEl Stargate	None
Memory Control	133 MHz SDR 266 MHz DDR 133 MHz QDR (March)	133 MHz QDR

Gigabit Ethernet MAC

- Applications
  - Routers, Switches, Repeaters, NICs
  - Prototype Gigabit MAC Controllers
  - Integrated Standard Gigabit Parts
- Runs at 125 MHz
- Requires 20K400E or Larger Device
- Consumes 3-6,000 Logic Cells
- Physical Transport Media Can be Copper or Optical
  - Optics Requires the 8b/10b Encoder/Decoder
- Configuration Options
  - GMII, 8B/10B, RMII & MII interface to the PHY
  - Flow Control for Full Duplex and Half Duplex Modes
  - 8B/10B based Auto-negotiation Options

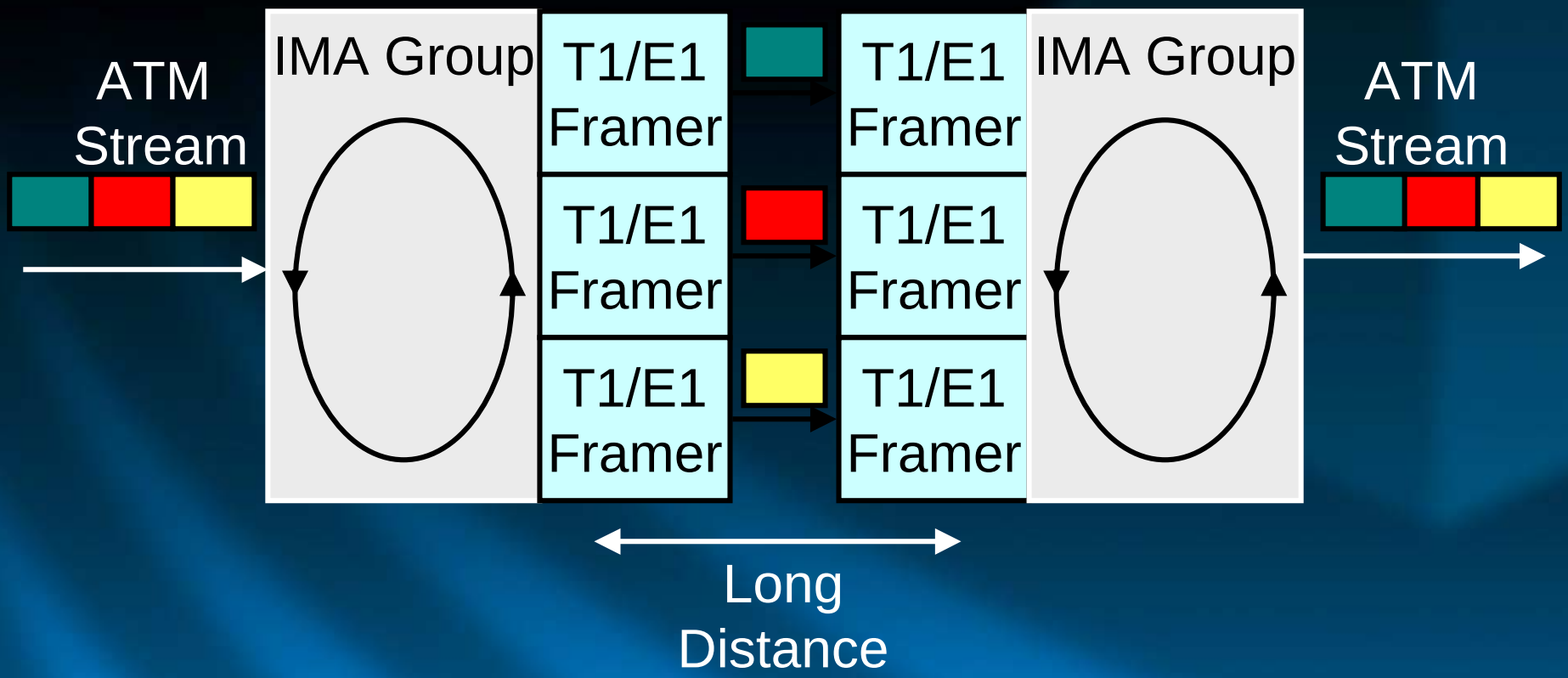
Gigabit MAC Product Comparison

Partner	Features	Interface	HDL	Verification	Resources	OpenCore
CoreEl	1000-Mbits/s Full Duplex Auto-Negotiation 8b10b Encoder/Decoder	32-bit Application Interface	VHDL	VHDL Testbench	Device: 20K400E LCELL: 2243 ESB bits: 13056	Yes
Stargate	10/100/1000-Mbits/s Auto-Negotiation 8b10b Encoder/Decoder Full/Half Duplex	9-bit Application Interface	Verilog	Verilog Testbench APEX Board	Device: 20K400E LCELL: 4715 ESBbits: 112440	Yes
SRTI	10/100/1000-Mbits/s 8b10b Encoder/Decoder RMON Module Full/Half Duplex	64-bit Application Interface EEPROM/ROM Interface Power Management Interface Auto-Negotiation Interface to PHY Auto-Negotiation Hardwire Interface	Verilog	Verilog Testbench	Device: 20K400E LCELL: 5877 ESB bits: 41600	Yes

What is IMA 1.1?

- Inverse Multiplexing and De-multiplexing for ATM Cell Streams
- Specification Defined by the ATM Forum
- Products are Tested by Organizations like UNH
- Converts ATM Layer Packets to T1/E1/DS3
- Target Applications
  - ATM Access Systems, DSLAMs

ATM Access System with IMA 1.1



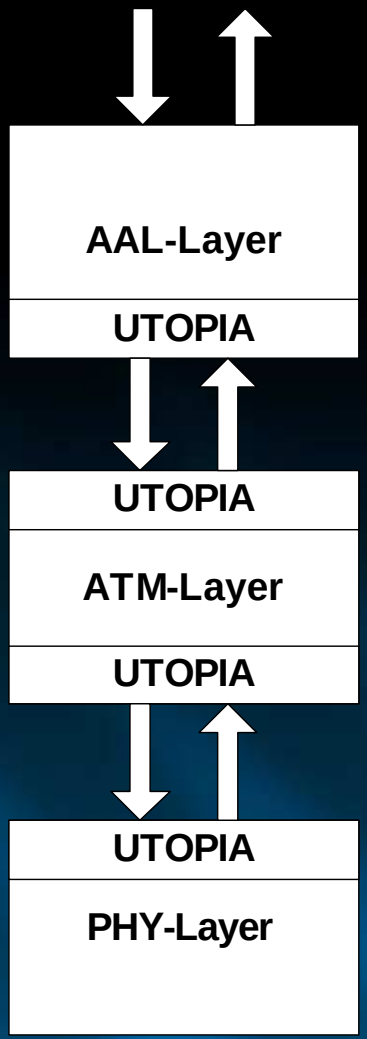
Comparing ModelWare and Apptel

- ModelWare
  - Current optimization is on 32 links, the largest possible
  - Implements Real-time critical functions in hardware
  - Therefore, consumes more PLD space
  - Implements house cleaning functions in software
  - Places less of a burden on Intel/Mot Processor in system
  - Requires one off-chip memory
- Applied Telecom
  - Spartan 2 solution requires use of Infineon's IWE8
  - Implements time critical functions in software
  - Requires cycles on the processor
  - Requires one off-chip memory

ModelWare IMA 1.1 Features

- Scalable to 32 Links, 16 Groups
- Flexible Grouping (any link to any group)
- Shared Architecture to Minimize Size
- Minimizes Required Software Interaction
- Supports Standard MPUs: Intel and Motorola
- Interface to PHY Layer over UTOPIA 2 Master
- Interface to ATM Layer over UTOPIA 2 Slave

UTOPIA Overview



- AAL Layer
  - Adaptation of Service
  - Segmentation and Re-assembly(SAR)
- ATM Layer
  - Header Management
  - Cell Switching
  - Traffic Management
- PHY Layer
  - HEC Checking
  - Scrambling/De-scrambling
  - Framing

UTOPIA 3 Slave

- Independent clocking for UTOPIA and Local interfaces >110MHz
- Multiple Bus Width (parameterized)
  - UTOPIA Bus width 8, 16, or 32 bits
  - Local Bus width 8, 16 or 32 bits
- Bus Width Tapering (parameterized)
  - 8-bit UTOPIA to 16 or 32 bit Local Bus
  - 16-bit UTOPIA to 32 bit Local Bus
- Targets APEX 20KE Family

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UTOPIA 3 Slave

- Optional parity generating/checking in transmit/receive direction
- Optional cell discard based on bad parity in the transmit direction
- Single or Multi- PHY mode
- Single or Multi- CLAV mode
- Variable cell length: 52 or 53 (8 bit) / 54 (16 bit) bytes long

UTOPIA 3 Features

- Bus Width Parameterized
  - Determined by Application
  - 8 bits = 394 Lcells, 3 ESB
  - 16 bits = 446 Lcells, 2 ESB
  - 32 bits = 626 Lcells, 12 ESB
- Optimized for APEX
  - Spec defines 104 MHz Operation
  - OpenCore Support, MegaWizard Support

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Megafunction Summary

- Megafunctions Are Critical for Large-Scale Design
- Cores from a Variety of Sources
  - Altera Provides MegaCore Functions
  - Over 107 Functions from 25 AMPP Partners
- OpenCore™ Program Allows Free Trial
- MegaWizard Plug-Ins Automate Integration